

## PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : SVCC  
LAYER 6 : BOT

### DB

#### QP/N

32ZM2PB0000  
33ZM1MA0010  
34ZM2TB0000  
35ZM2LB0000  
3BZM2BB0000

### USB&PCIE PORT

USB Port#	Destination
0	Right top
1	Right bottom
2	Left side
3	Bluetooth
4	Camera
5	Touch Screen
6	Mini-WLAN
7	Mini-WWAN

PCI-E Port#	Destination
PCI-E-1	Mini-WWAN
PCI-E-2	Mini-WLAN
PCI-E-3	Card reader
PCI-E-4	LAN

### Power

+3.3V\_ALW/+5V\_ALW(MAX17020)  
PAGE 36

+1.8VSUS(RT8207)/  
+VTT\_MEM  
PAGE 35

+VCC\_CORE (MAX8796)  
PAGE 33

CHARGER (MAX8731A)  
PAGE 32

+VCC\_GFX\_CORE(RT8209A)  
PAGE 31

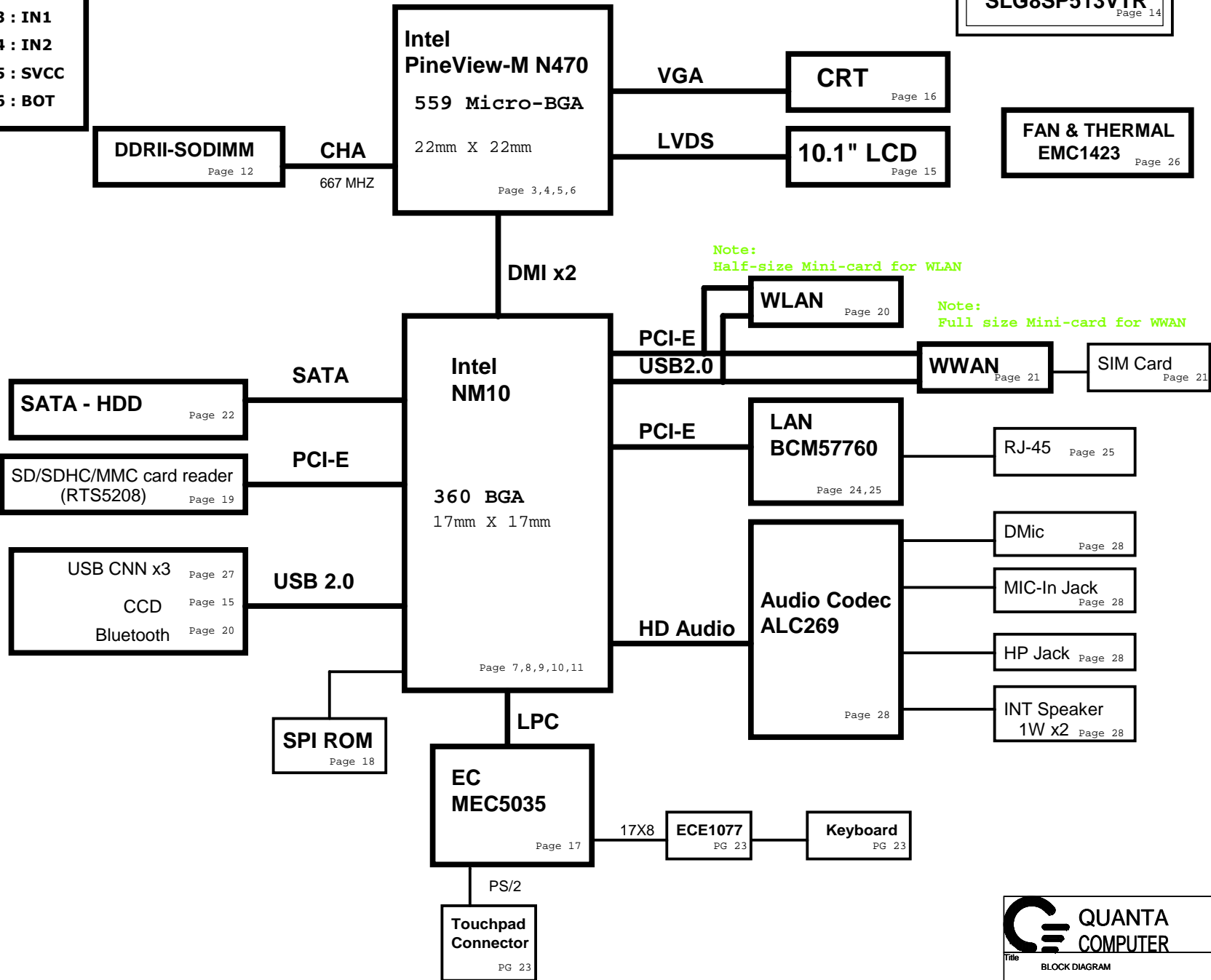
+VCCP(RT8209A)/  
+VCC1.5(RT9018B)  
PAGE 34

# ZM2 BLOCK DIAGRAM

## CLOCK GEN

SLG8SP513VTR  
Page 14

FAN & THERMAL  
EMC1423  
Page 26










## Table of Contents

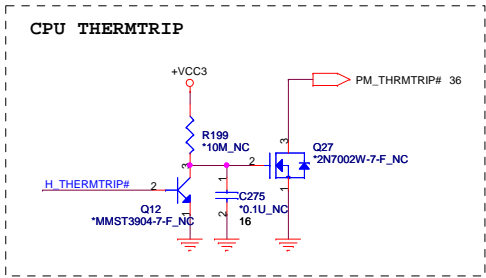
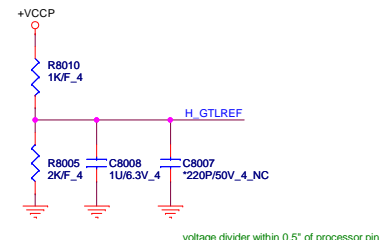
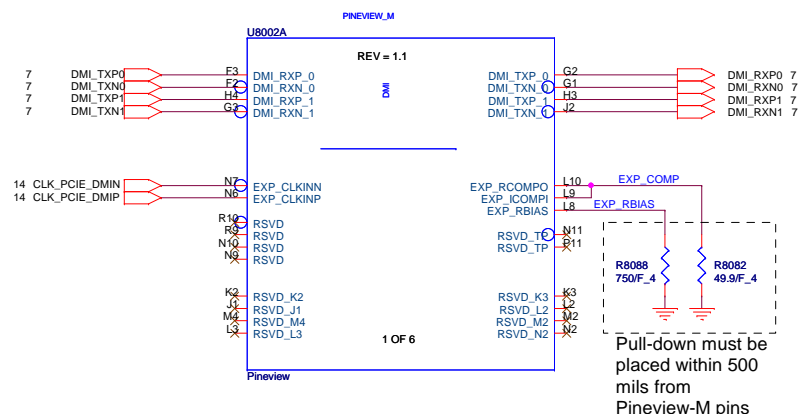
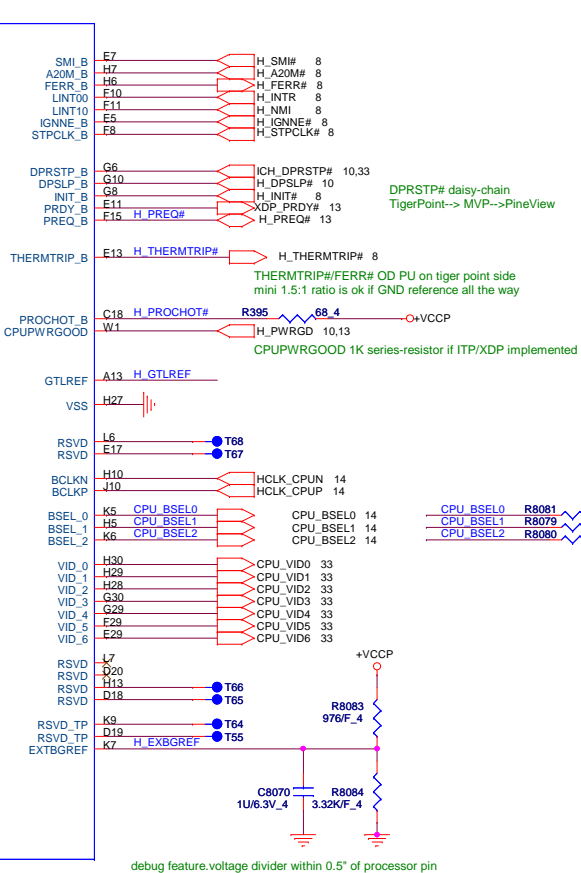
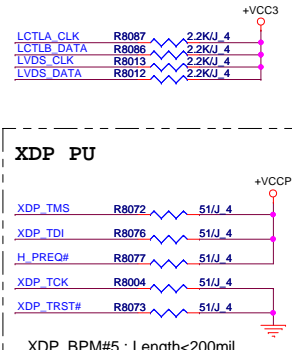
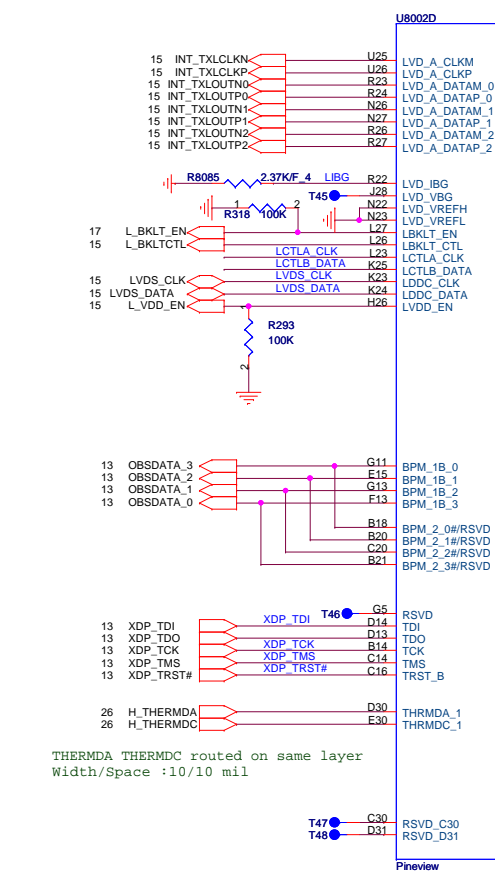
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-6	Prineview
7-11	TGP
12	DDRII SO-DIMM(200P)
13	XDP Debug Port
14	Clock Generator
15	LCD Conn. ,CCD,TouchScr
16	CRT Conn
17	SIO(MEC_5035)
18	FLASH/RTC
19	Card Reader-RTS5208
20	Mini Card(WLAN)
21	MINI-WWAN
22	SATA (HDD)
23	KB/TP
24	LAN POWER
25	LAN(BCM57760)
26	FAN & Thermal
27	USB
28	Audio CODEC(ALC269)
29	LED & SWITCH
30	System Reset Circuit
31	VGA Power
32	Charger (MAX8731A)
33	CPU(MAX8796)
34	1.05VCCP & VCC1.5
35	1.8VSUS & 0.9VTT (TPS51116)
36	3.3V/5V_ALWPower
37	RUN Power Switch
38	DCIN&Batt
39	PAD& SCREW
40	EMI CAP
41	SMBUS BLOCK
42	Power Block Dianram
43	Port Mapping

## Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	15,18,,32,33,35,36,40	MAIN POWER		S0~S5
+VCCRTC	+3.0V~+3.3V	10,11,17,18	RTC		S0~S5
+3.3V_ALW	+3.3V	17,18,24,25,29,31,32,34,35,36,37,38,40	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	23,24,29,34,35,36,37,38	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	15,24,36,37	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	24,25,40	LAN POWER	LAN_PWR_ON	
+5V_SUS	+5V	24,27,29,33,37,40	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	15,24,29,30,33,34,37	SLP_S5# CTRLD POWER	SUS_ON	
+1.8VSUS	+1.8V	4,5,12,13,34,35,37	SODIMM POWER	SUS_ON	
+VTT_MEM	+0.9V	12,13,35,37	SODIMM POWER	RUN_ON	
+VCC1.8	+1.8V	5,37		RUN_ON	
+VCC5	+5V	11,15,16,22,23,26,28,29,37,40	SLP_S3# CTRLD POWER	RUN_ON	
+VCC3	+3.3V	3,5,6,8,9,10,11,12,13,14,15,16,17,19,20,21,22,24,25,26,28,29,33,37,40	SLP_S3# CTRLD POWER	RUN_ON	
+VCC1.5	+1.5V	5,7,11,20,21,34,37,40	CALISTOGA/ICH8 POWER	RUN_ON	
+VCCP	+1.05V	3,5,8,11,34,40	CPU/CALISTOGA/ICH8 POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	5,33,40	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	15	LCD Power	LCDVCC_TST_EN & ENVDD	
+VCHGR	+10V~+17V	32,38	MAIN BATTERY	CHG_PBATT	

GND PLANE	PAGE	DESCRIPTION
 GNDA_CHG	35	
 GND_1.05V	36	
 AGND_DC/DC	38	
 GND POWER	33	
 AGND_DDR		
 PM6686TR		
 GND	ALL	

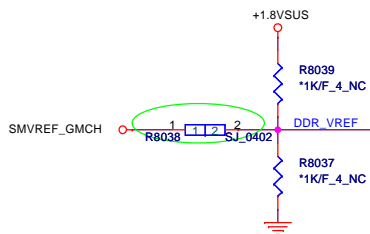
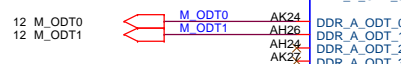
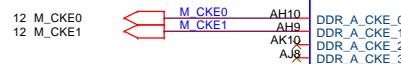
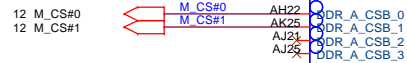
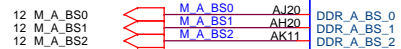
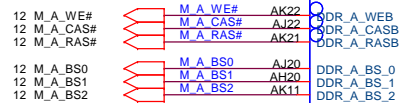
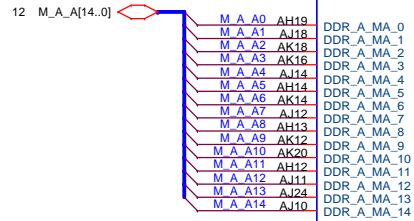




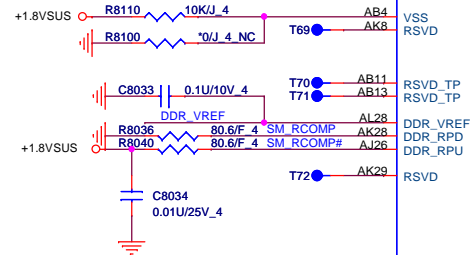
U8002B

PVIEW\_M

REV = 1.1



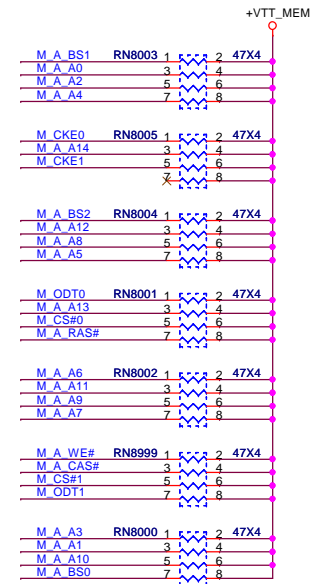
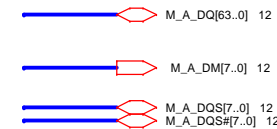
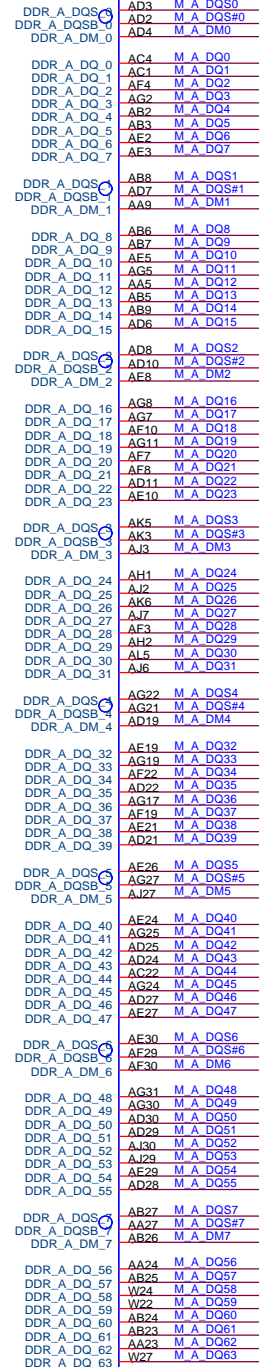
1C: reserve for ES1(WW10 MOW)



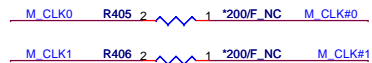
DDR\_A

2 OF 6

Pineview



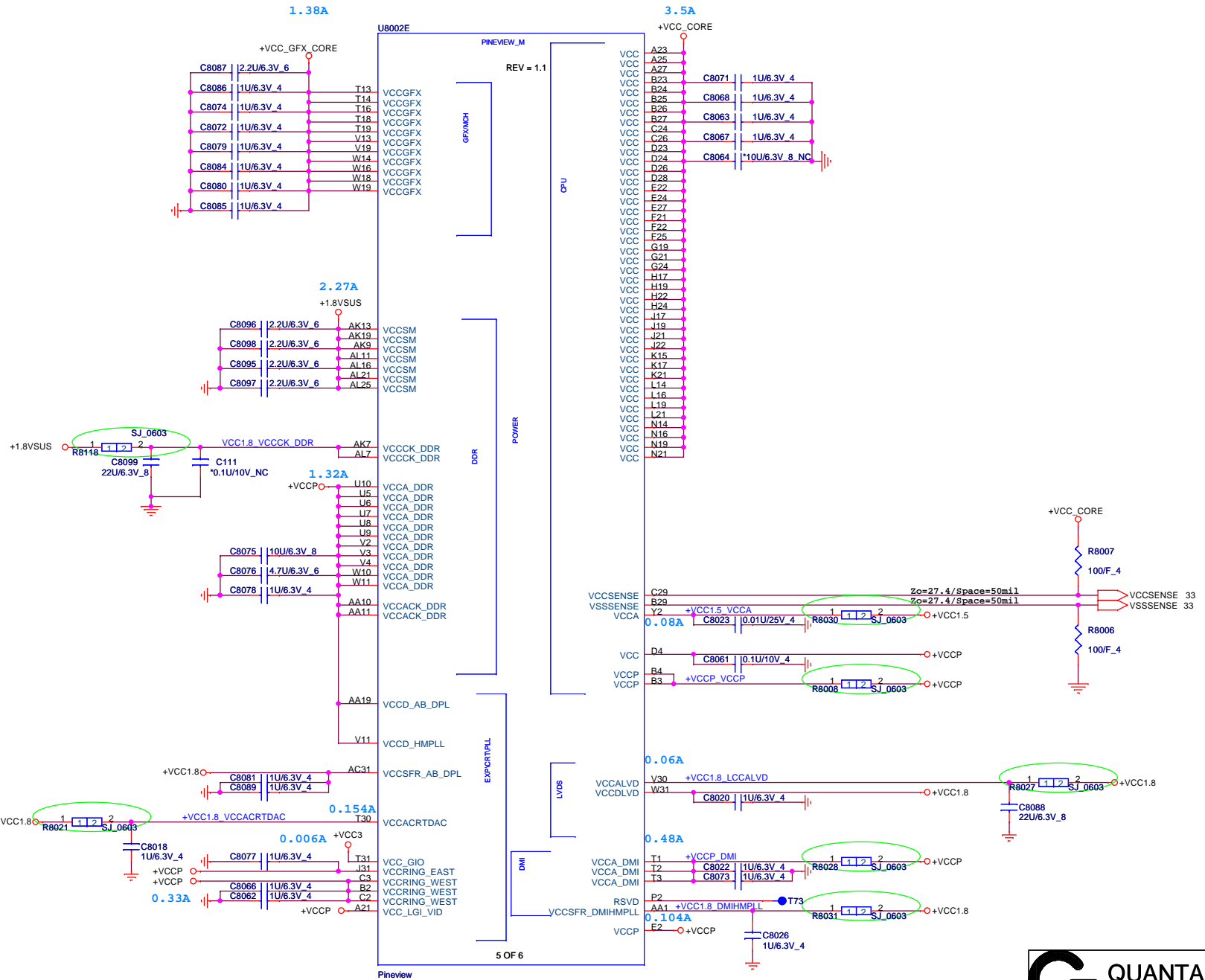
10/21 For EMI Reserve

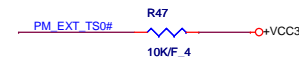
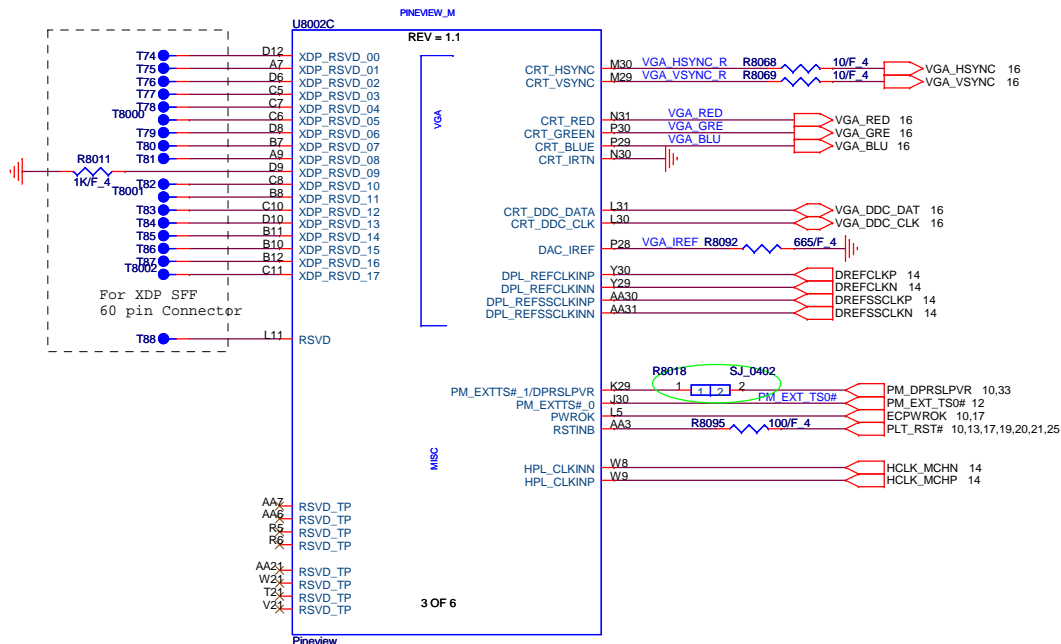
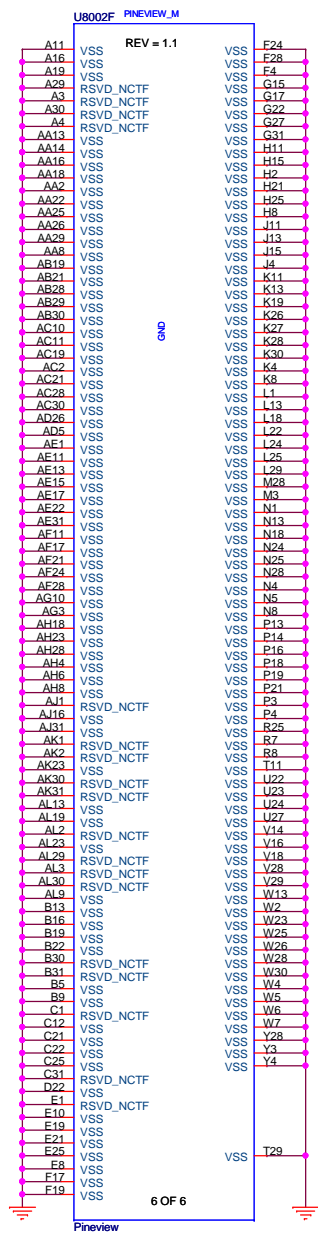
Title  
DDR2Size  
Document Number  
ZM2

Date: Wednesday, March 10, 2010

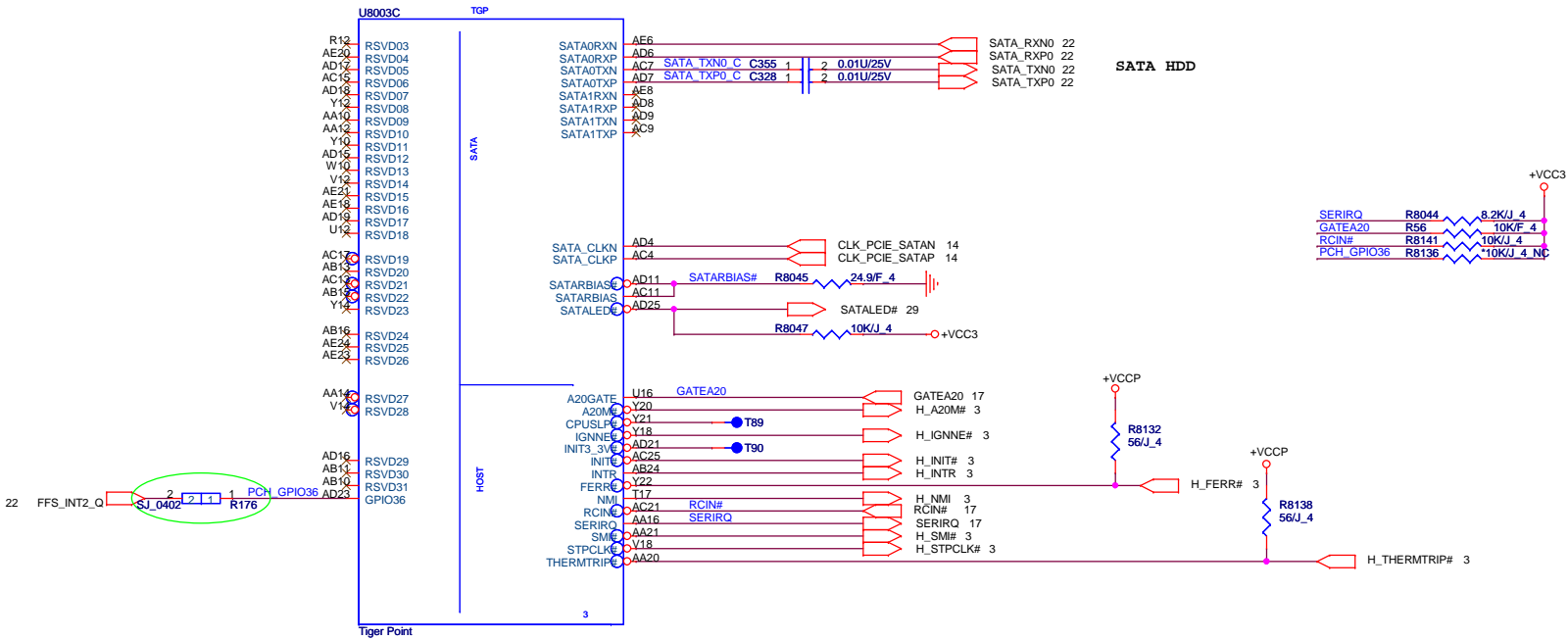
Sheet 4 of 43

Rev D

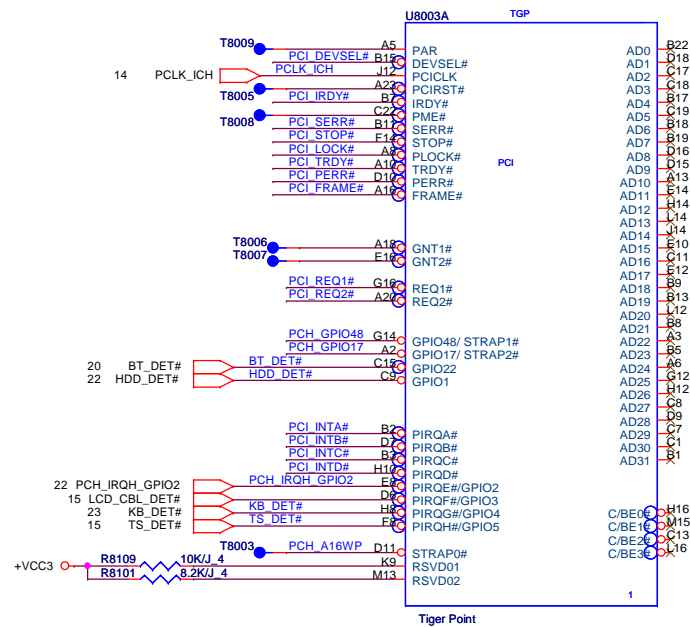


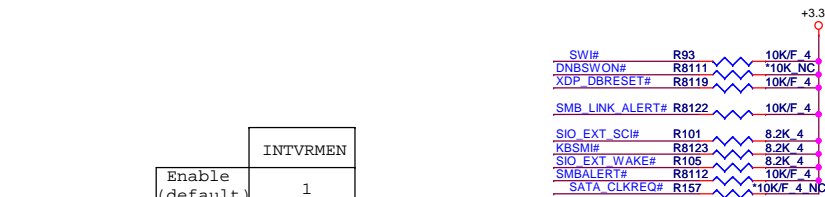
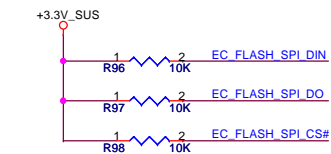
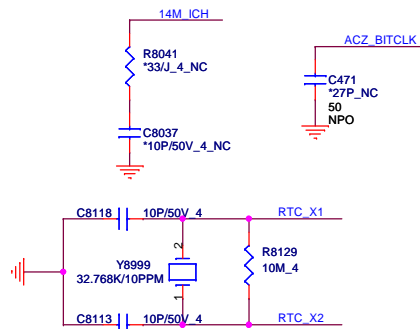




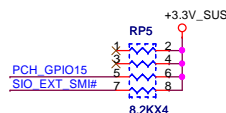
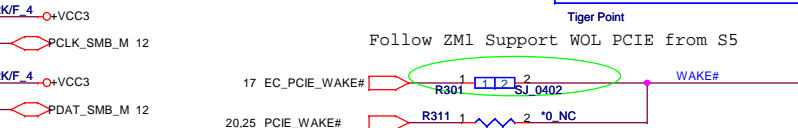




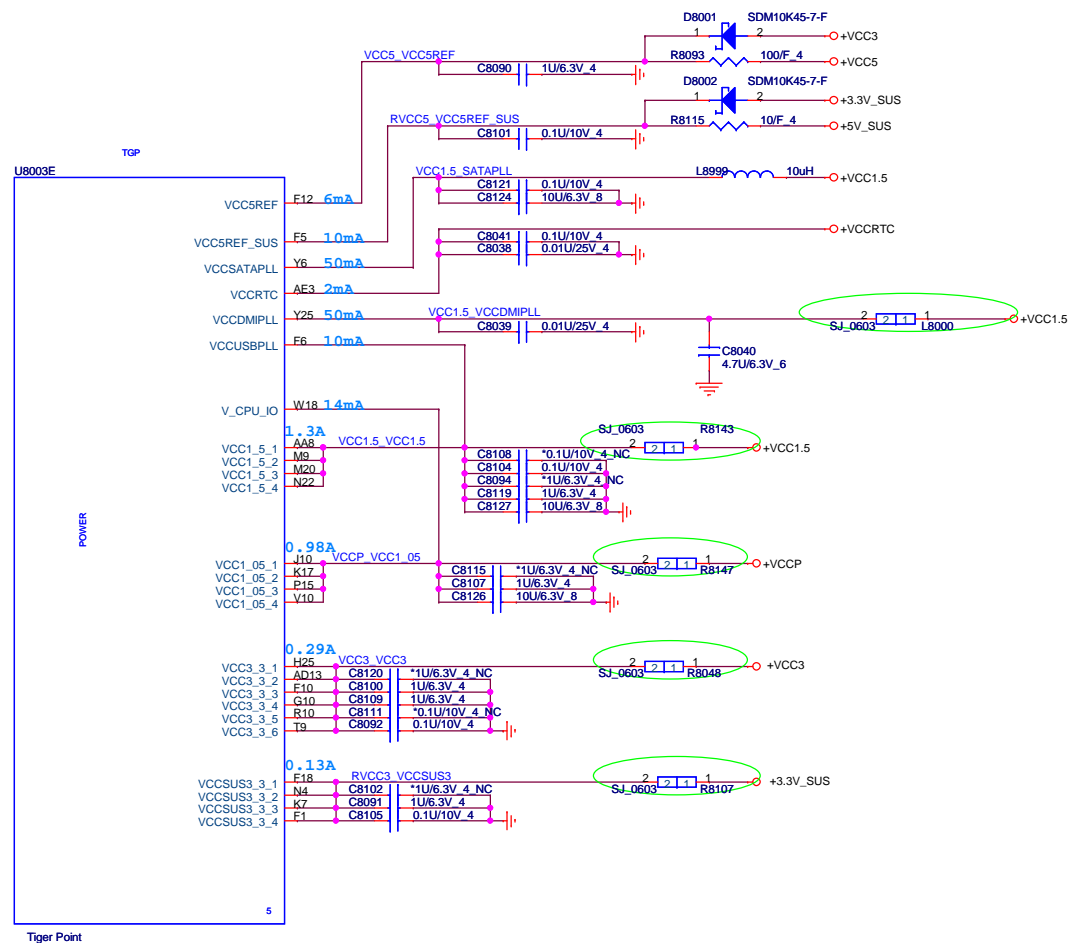
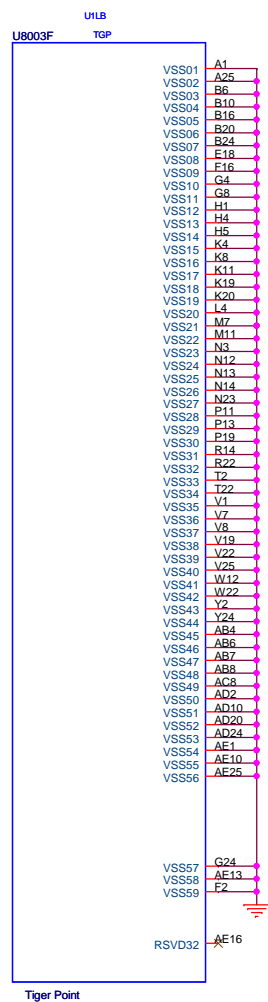




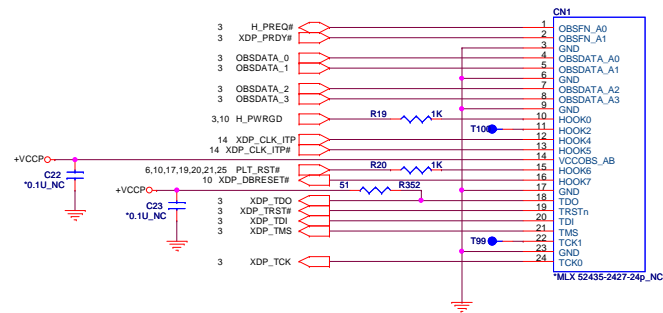
ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	★ 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

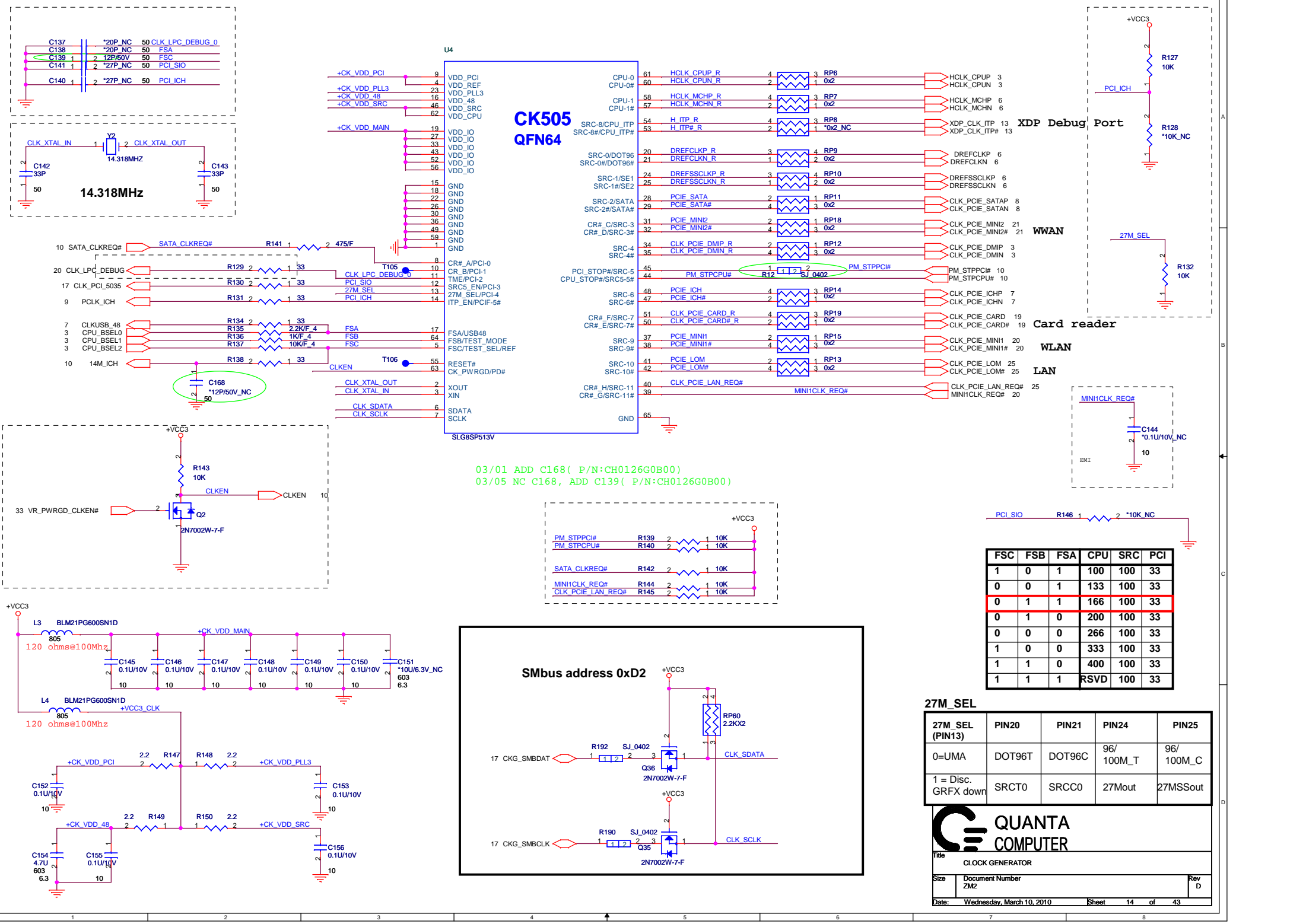


Date: Wednesday, March 10, 2010 Sheet 10 of 43









CK505  
QFN64

03/01 ADD C168( P/N:CH0126G0B00)  
03/05 NC C168, ADD C139( P/N:CH0126G0B00)

SMBus address 0xD2

WDP Debug Port

WWAN

Card reader

WLAN

LAN

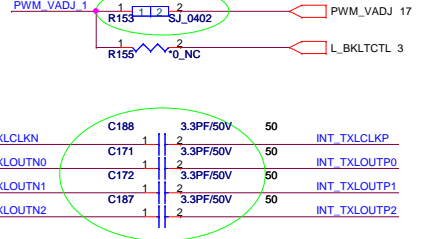
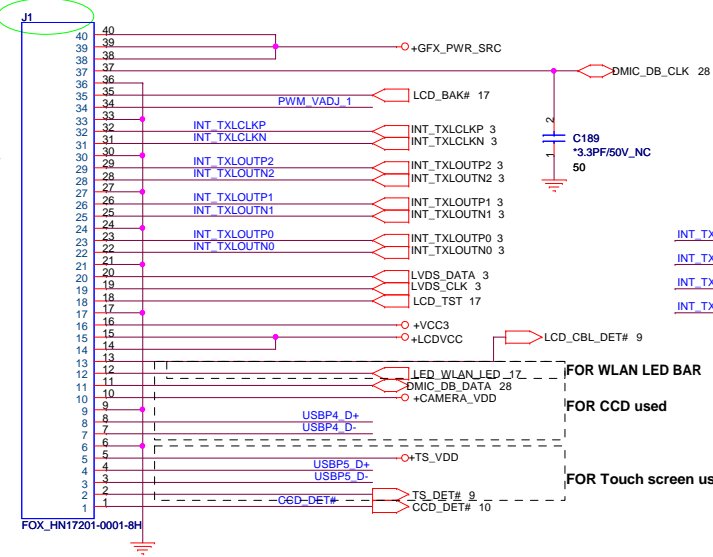
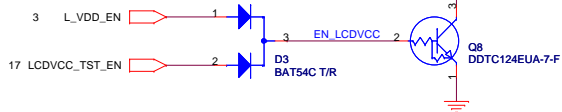
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M\_SEL

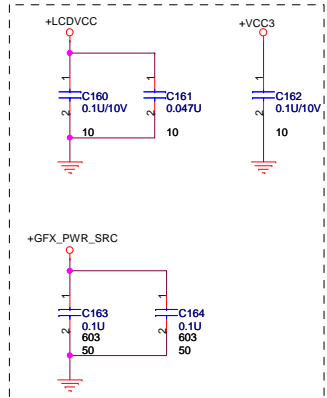
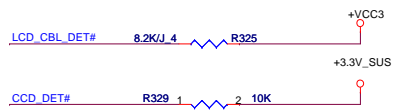
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



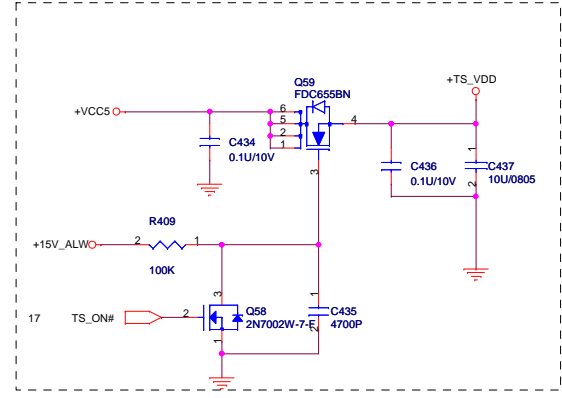
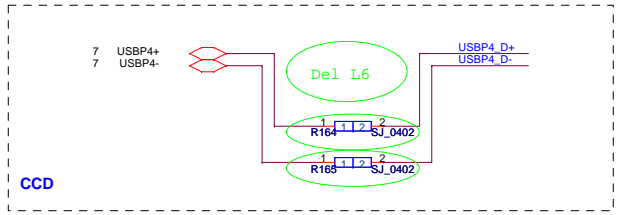
Support the new imbedded diagnostics.



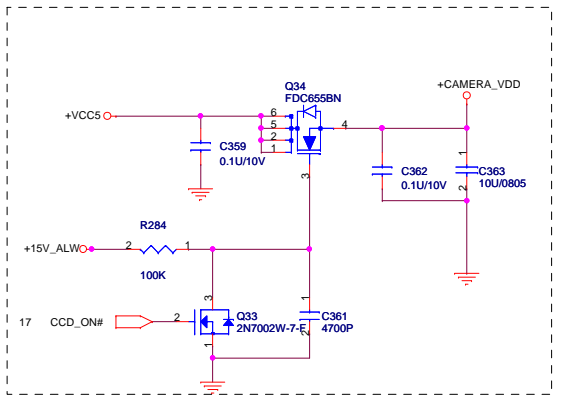
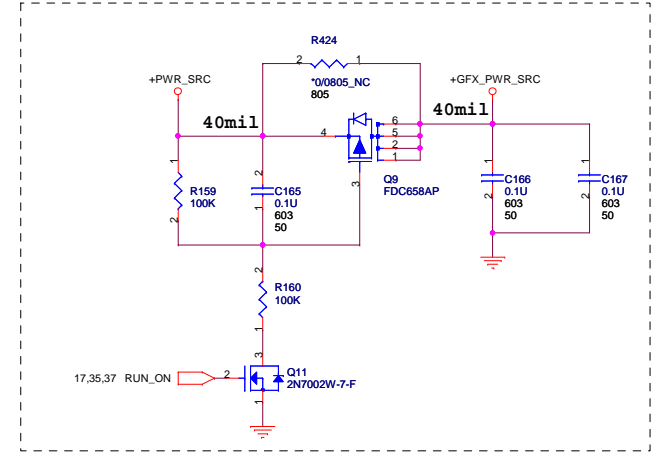
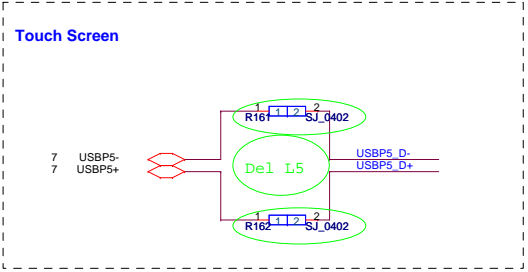
03/01 ADD C171,C172,C187,C188( P/N:CH-333B0B00)  
03/02 Change J1 P/N from DFHD40MR017 to DFHD40MR029

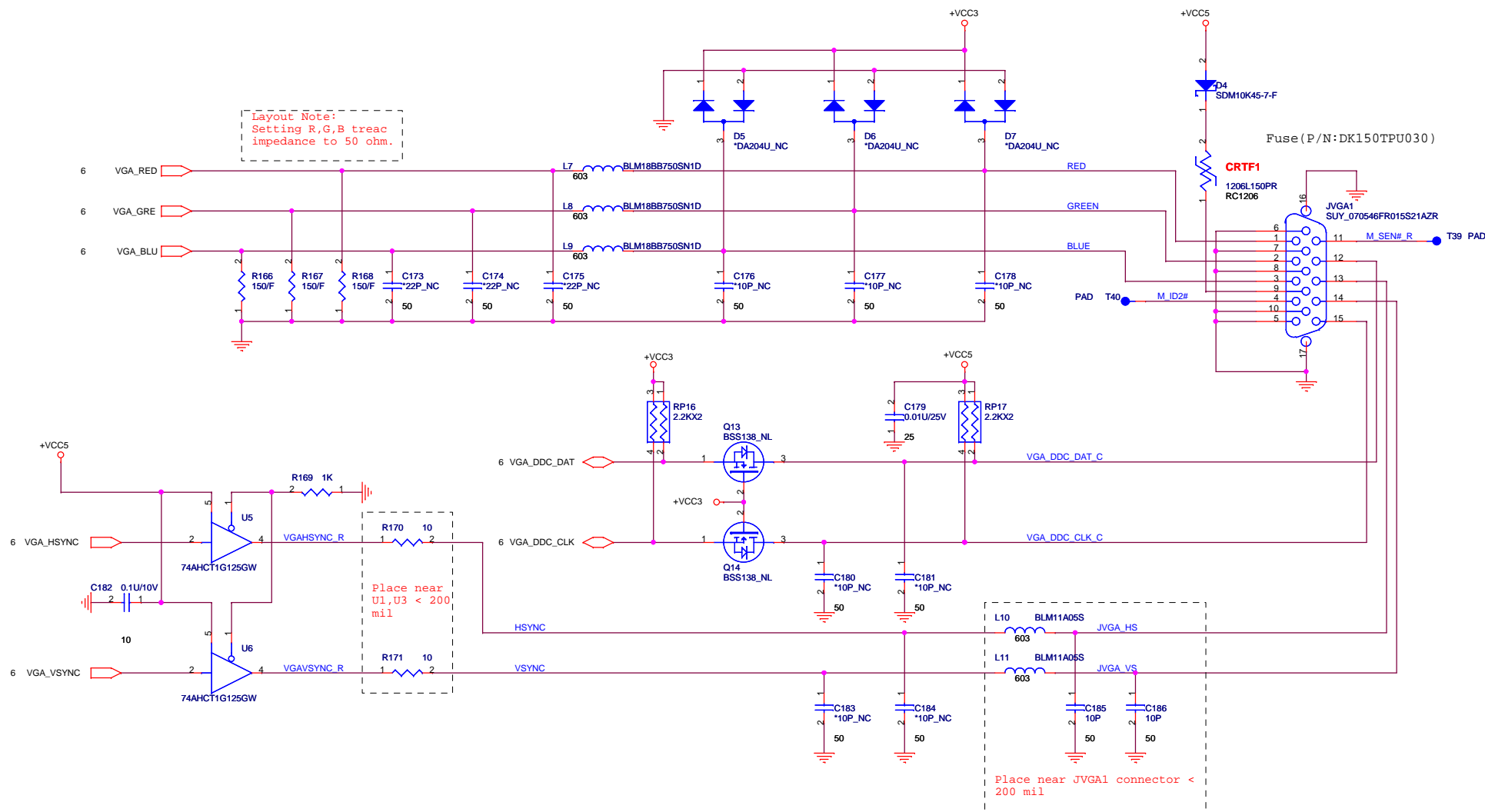


CCD



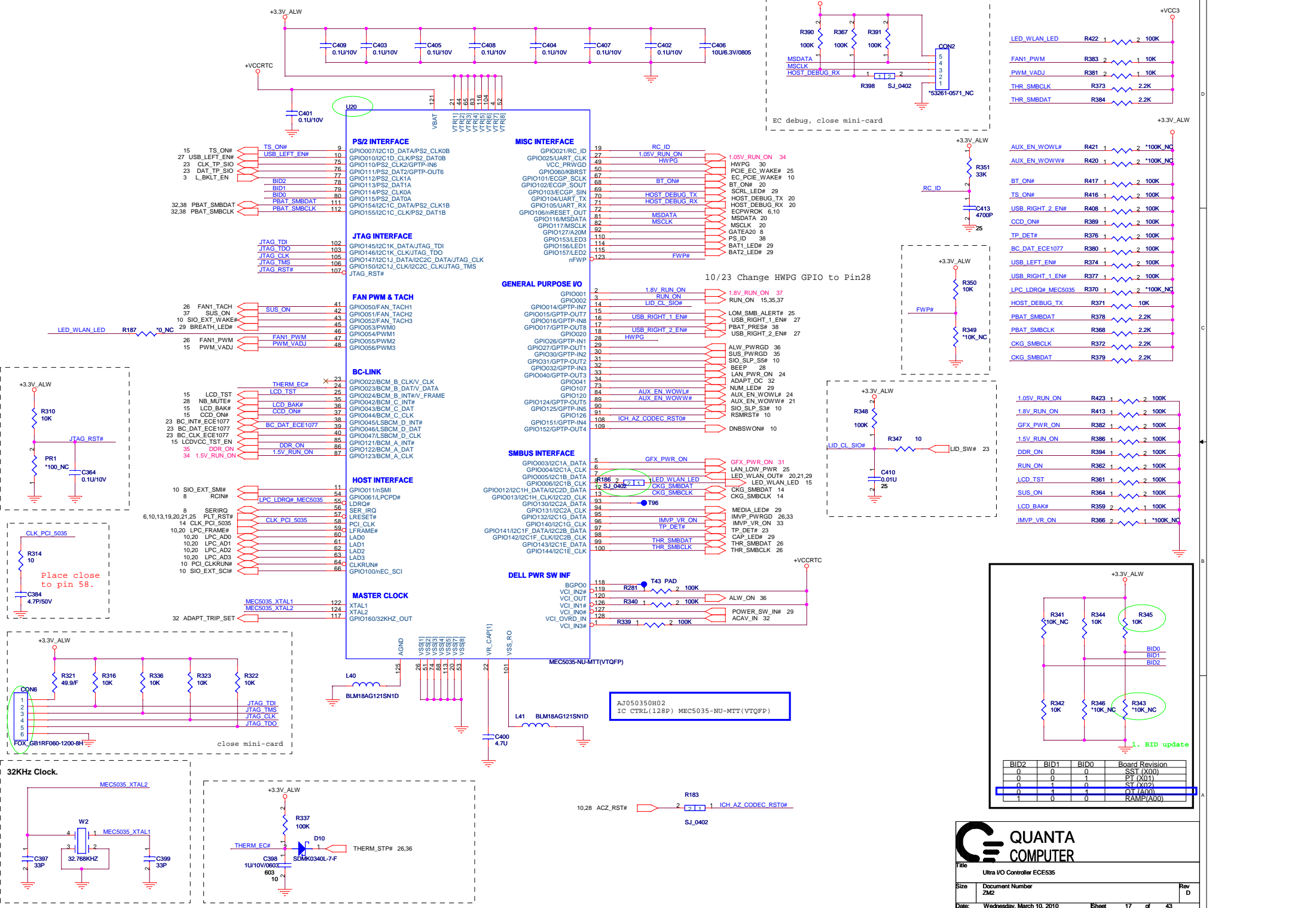
Touch Screen







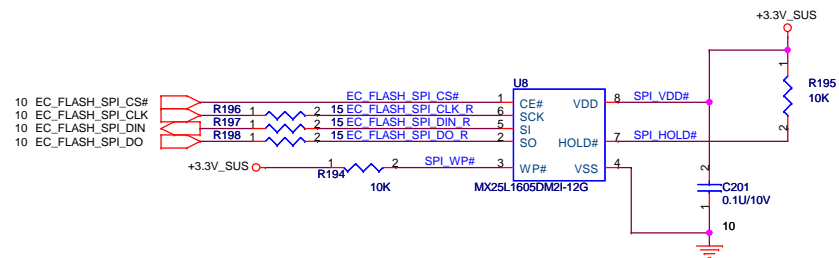
03/01 Change U20 P/N from AJ050350H01 to AJ050350H02.  
03/02 Change CON6 P/N from DFFC06FR022 to DFFC06FR054



BID2	BID1	BID0	Board Revision
0	0	0	SST (X00)
0	0	1	PT (X01)
0	1	0	ST (X02)
0	1	1	ST (A00)
1	0	0	RAMP(A00)



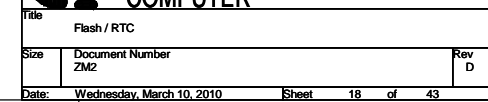
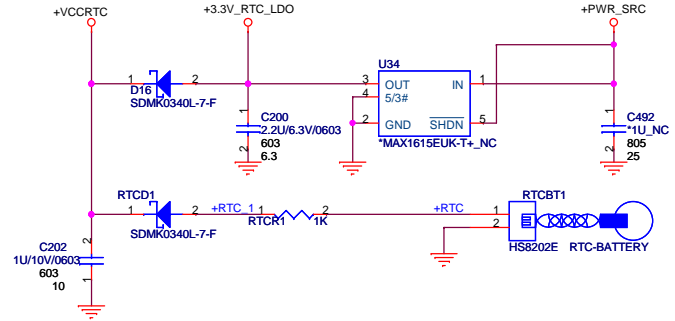
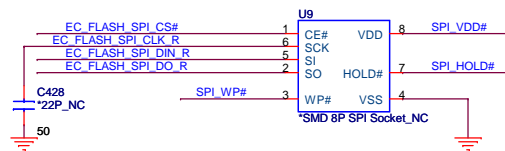
## SPI ROM Socket



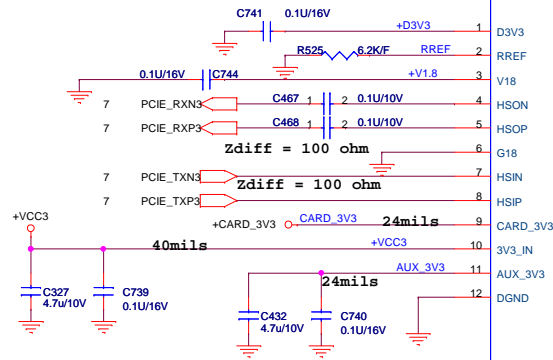
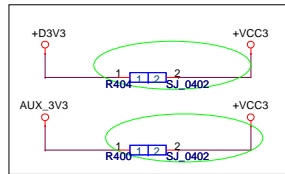
The diagram shows the SPI connection to U9 (SMD 8P SPI Socket\_NC). The connections are as follows:

- EC\_FLASH\_SPI\_CS# (Pin 1) connects to CE# (Pin 8).
- EC\_FLASH\_SPI\_CLK\_R (Pin 6) connects to SCK (Pin 5).
- EC\_FLASH\_SPI\_DIN\_R (Pin 5) connects to SI (Pin 2).
- EC\_FLASH\_SPI\_DO\_R (Pin 2) connects to SO (Pin 3).
- SPI\_WP# (Pin 3) connects to W/P# (Pin 4).
- VDD (Pin 8) connects to SPI\_VDD#.
- HOLD# (Pin 7) connects to SPI\_HOLD#.
- VSS (Pin 4) connects to ground.

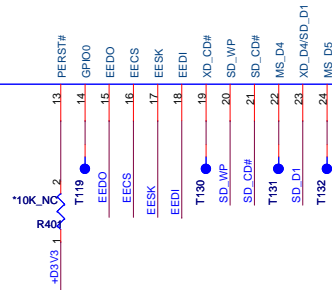
A capacitor C428 (22pF) is connected between the CS# line and ground. The component is labeled "SMD 8P SPI Socket\_NC".



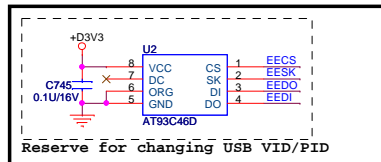
03/01 Del C326 for ASF issue  
03/10 Del C326,R403 Location



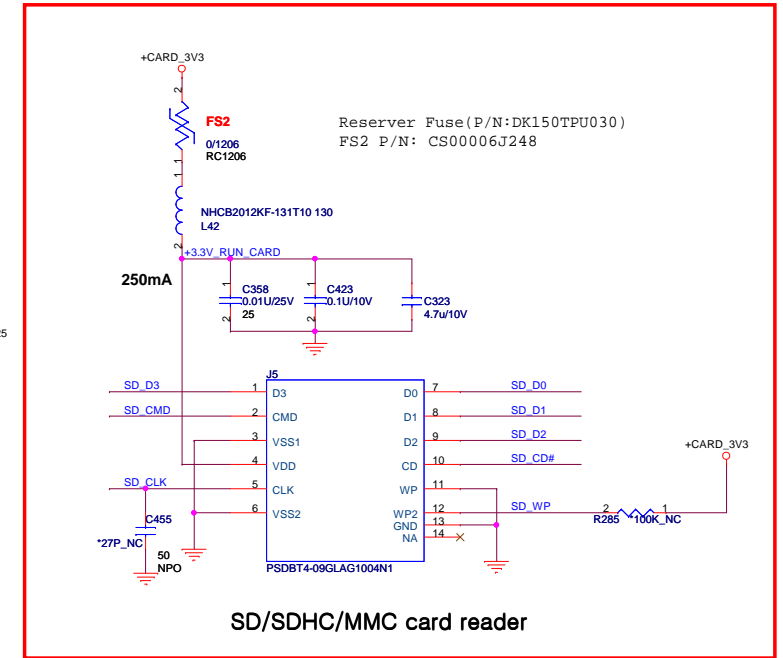
**RTS5208\_48p**



Need update EEPROM Footprint



**EEPROM**

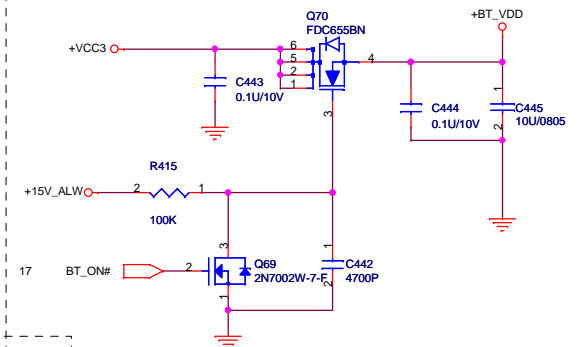


**SD/SDHC/MMC card reader**



[illegible]

<b>Non-iAMT</b>	T49	PAD	
	T50	PAD	
	T51	PAD	

[illegible]

WLAN\_RADIO\_OFF# 2 1 WLAN\_RADIO\_DIS# 10

D18  
SDMK0340L-7-F

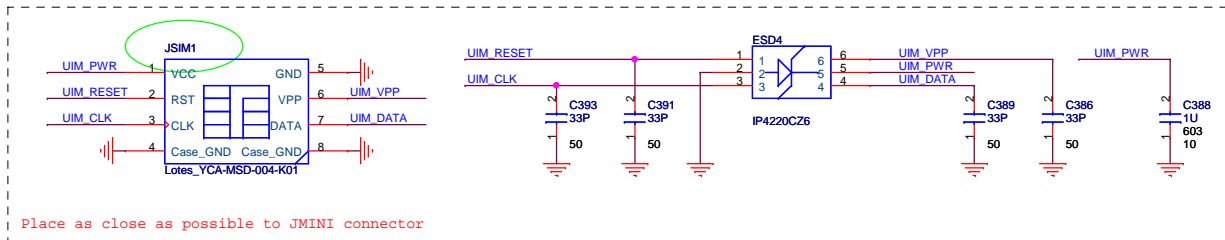
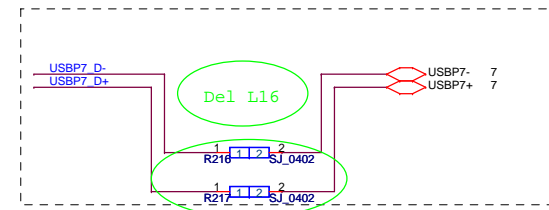
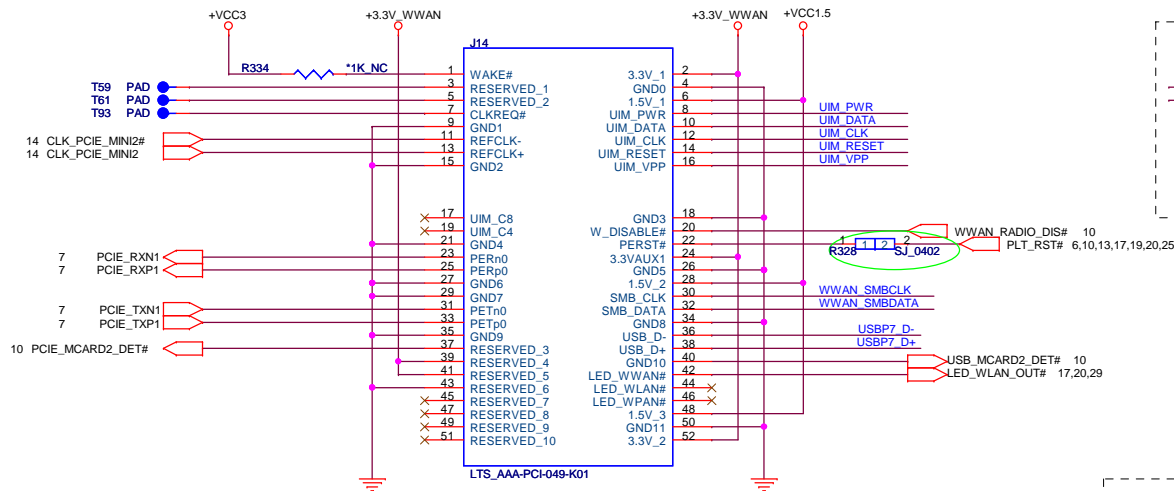
Bluetooth

	80 port	EC Debug
	Add R208,R209,R210, R211,R212,R214,R215	Add R356,R223,R357
17	NC R356,R223,R357	NC R208,R209,R210, R211,R212,R214,R215

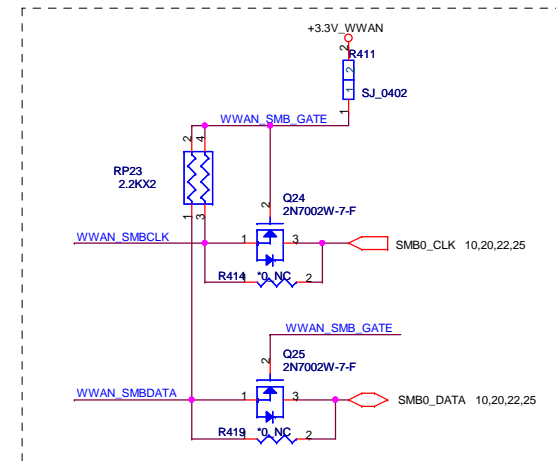
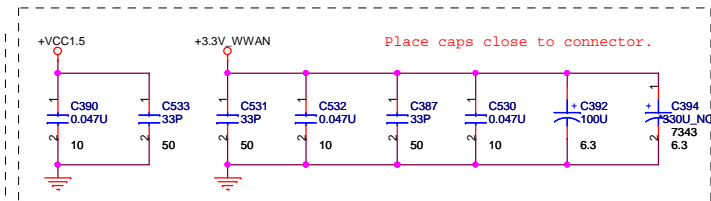
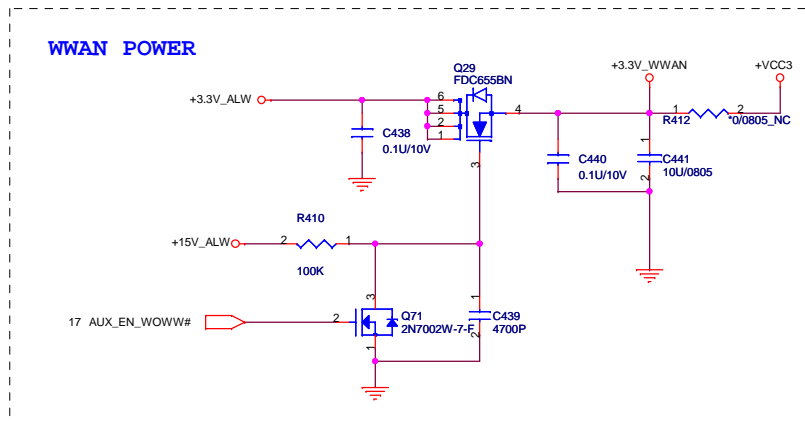


Title			
MDC CONN.			
Size	Document Number		Rev
	ZM2		D
Date:	Wednesday, March 10, 2010		Sheet 20 of 43

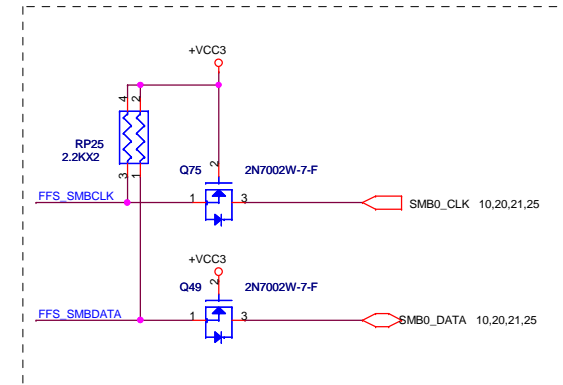
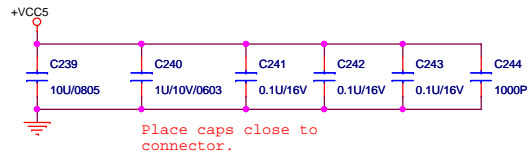
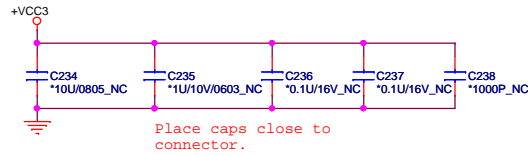
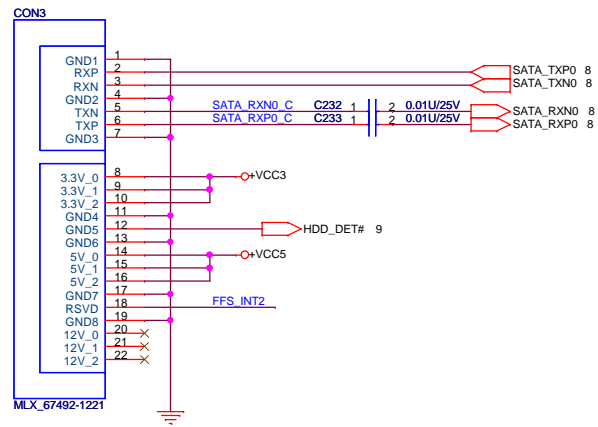
# MiniCard WWAN connector



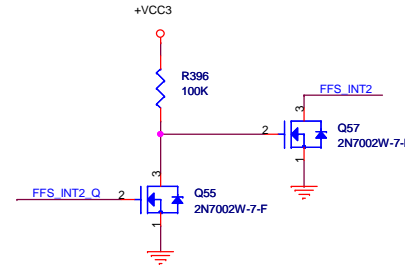
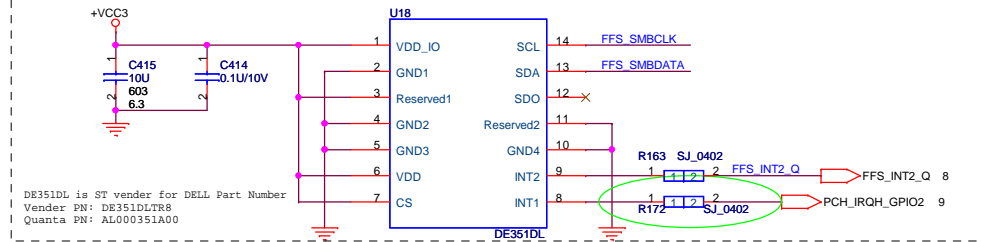
03/02 Change JSIM1 P/N from DG006000020 to DG006000031

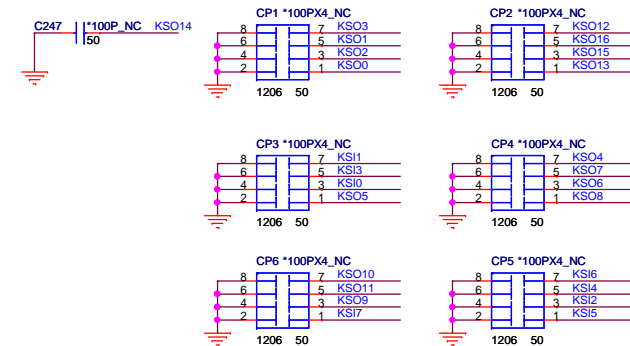
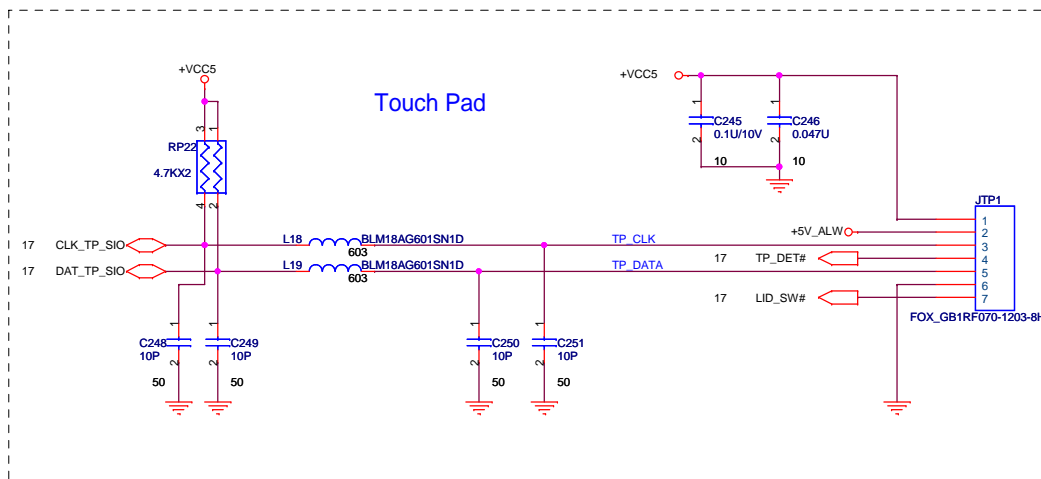


## SATA HDD Connector.



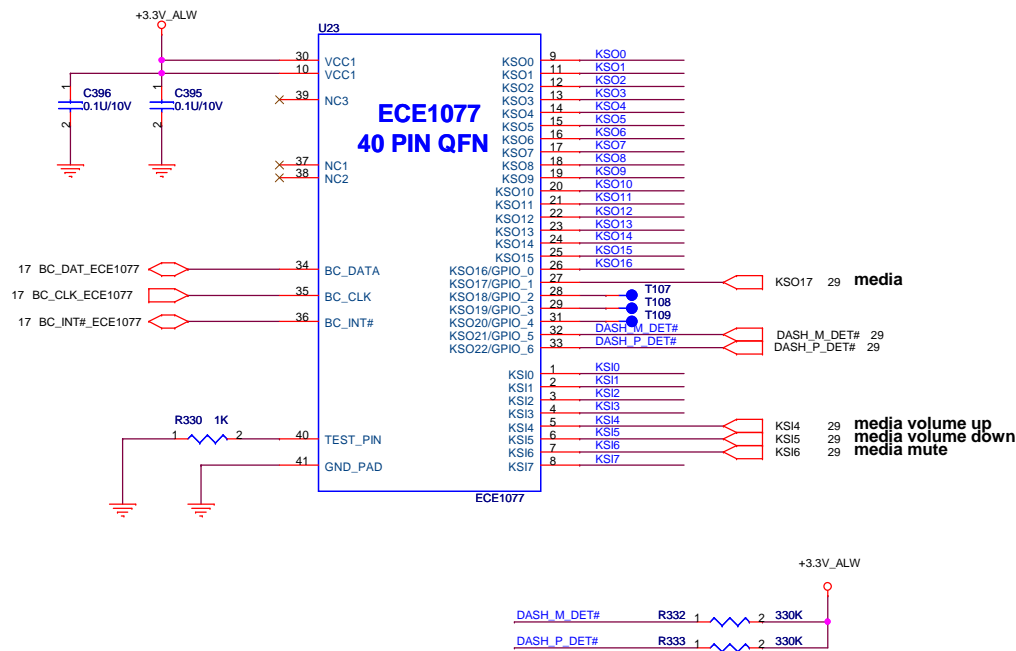
### 3-axis Fall Sensor (HDD data protector)



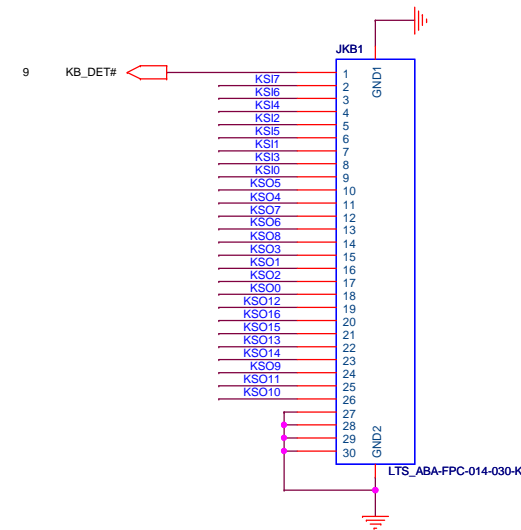


100P CAPS CLOSE TO JKB1

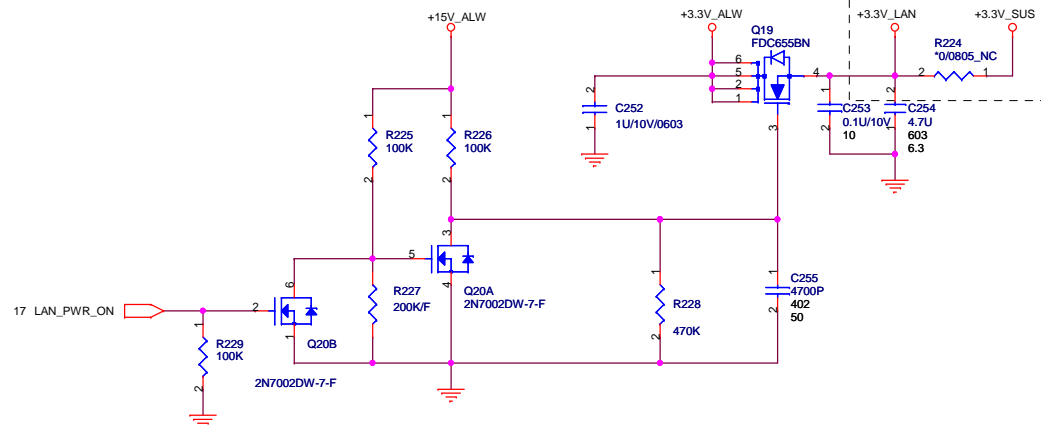
## Keyboard Scan Extension



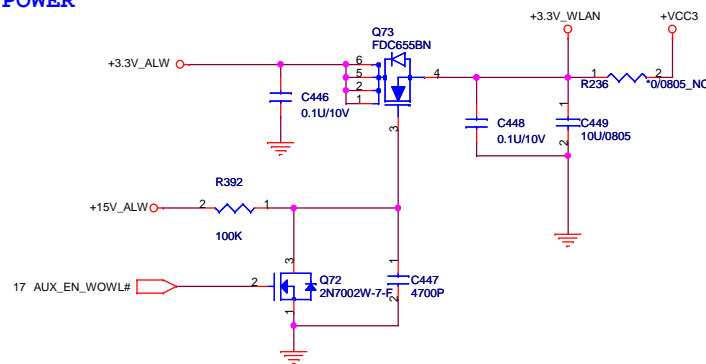
## KEYBOARD CONNECTOR



# Support Wake on LAN on S5.

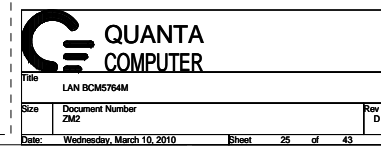


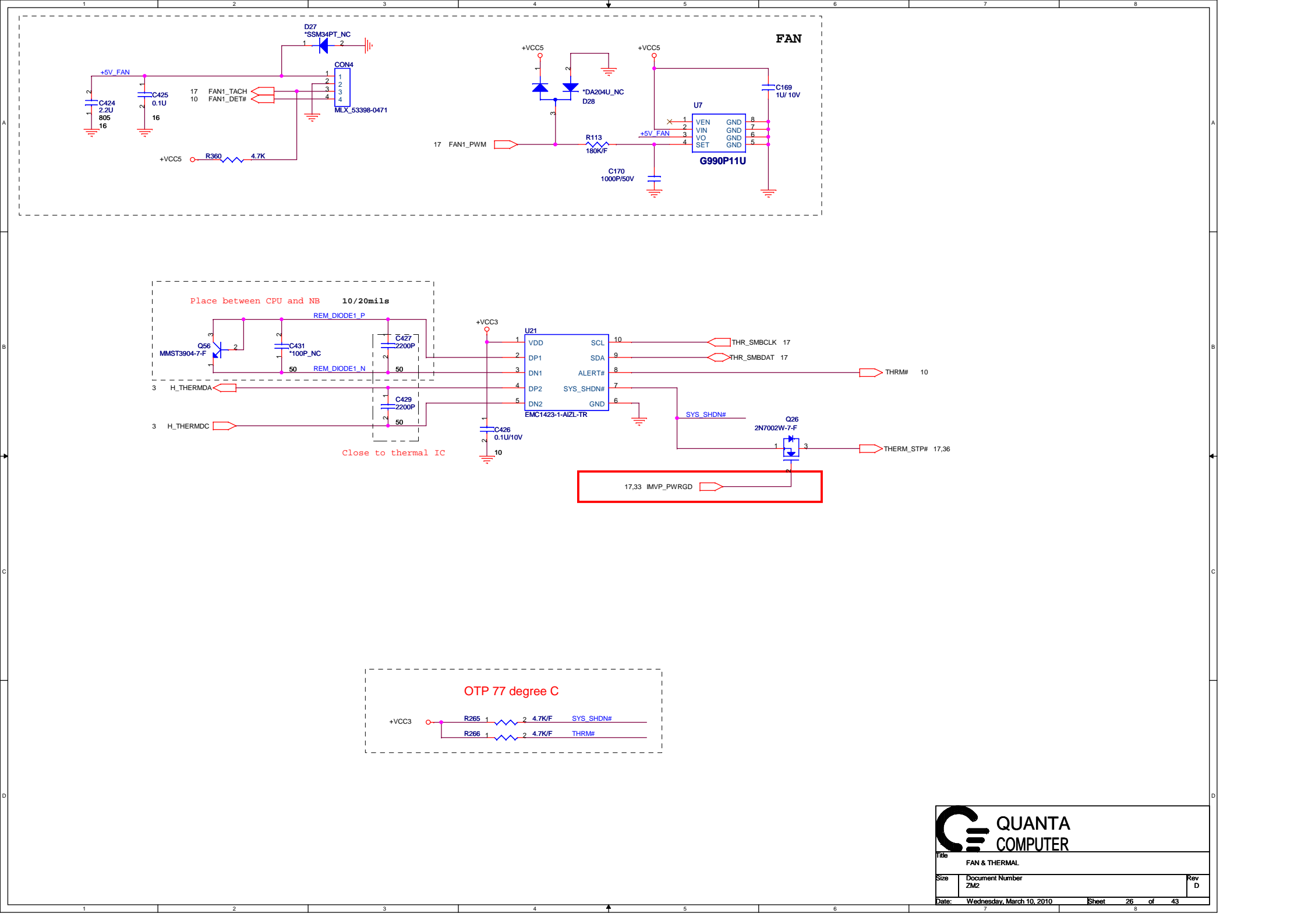
# WLAN POWER



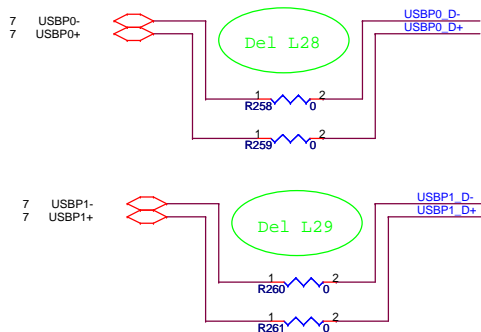
Title			LAN POWER
Size	Document Number	Rev	
	ZM2	D	
Date:	Wednesday, March 10, 2010	Sheet	24 of 43





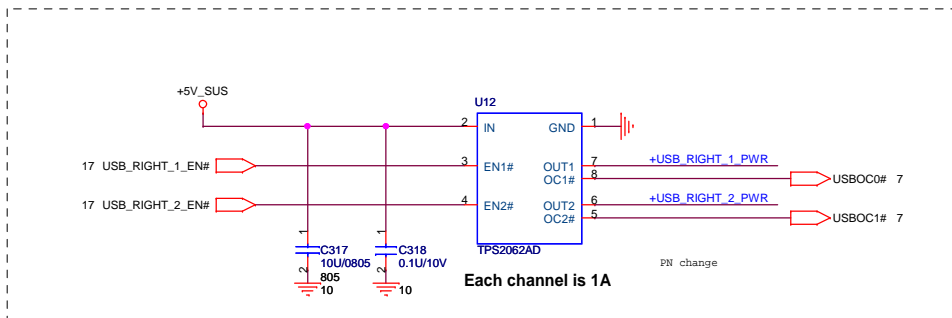
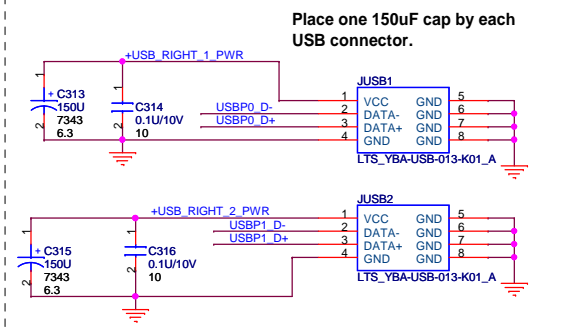
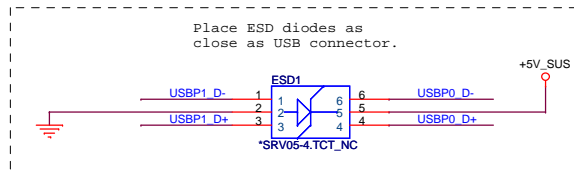


External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

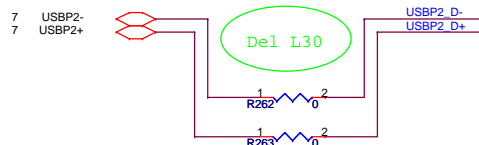


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

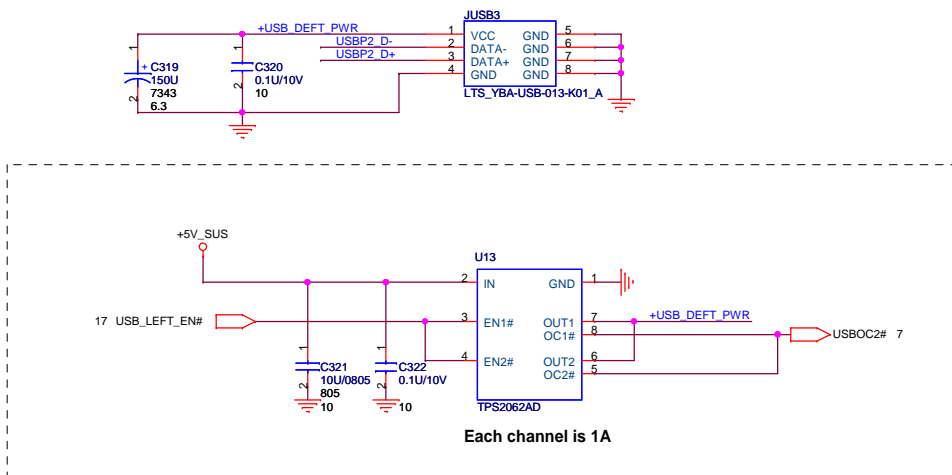
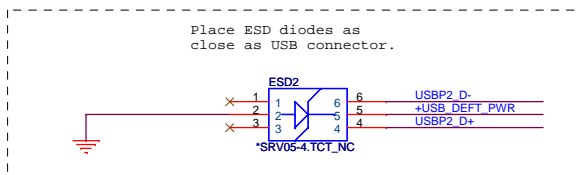
## USB Right Side x2



## USB Left Side



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



```
03/01 Change CN3,CN4 Footprint from audio-jas33l-10lwy0x-7f-5p-h
to audio-jas33l-10lwy0x-7f-5p-v
03/01 Add C433,C354(P/N:CH0126G0B00),
AddR407,R282(P/N:CS00002JB38)
```

\*NOTE: ALC269\_VB type add the LDO circuit in IC

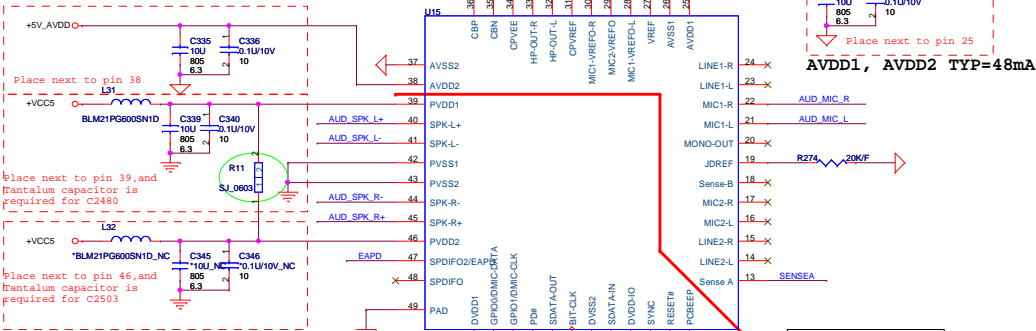
PIN NAME	R425	R375	R369	C417	CODEC IC
28 MIC1_VREF0-L			POP	NC	ALC269 VA
31 CPVREF	POP	NC			

PIN NAME	R425	R375	R369	C417	CODEC IC
28 MIC1_VREF0-L			NC	POP	ALC269 VB
31 CPVREF	NC	POP			

VA type: PIN28 as Bias Voltage for MIC1 Jack  
PIN31 connect to analog ground

VB type: PIN31 as Bias Voltage for MIC1 Jack  
PIN28 connect capacitor to analog ground

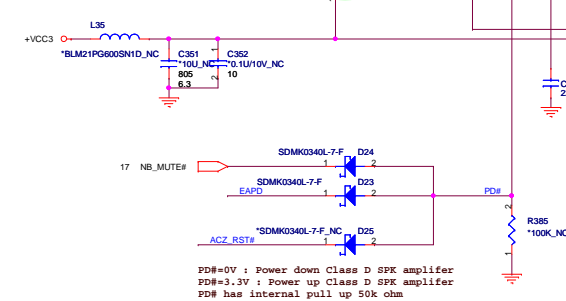
AVDD1, AVDD2 TYP=48mA



Analog Plane

Digital Plane

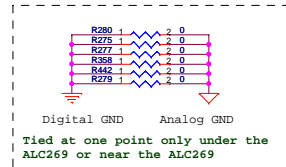
DVDD & DVDD-IO TYP=50mA



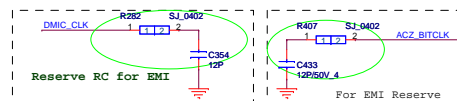
<<Attention>>

For power\_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :

1. If you want the system make warning signal after power on , please let EC\_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let the EC\_MUTE# Low. (The programming is different from before . )



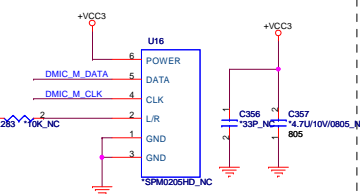
Tied at one point only under the  
ALC269 or near the ALC269



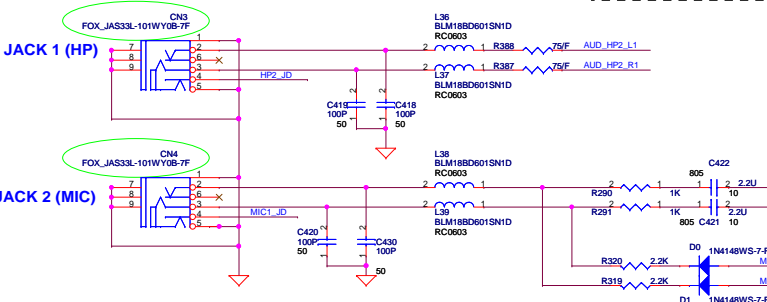
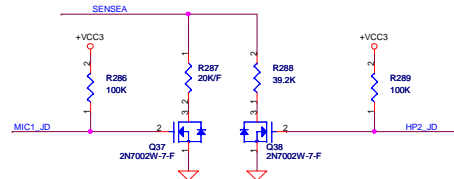
Reserve RC for

For EMI Reserve

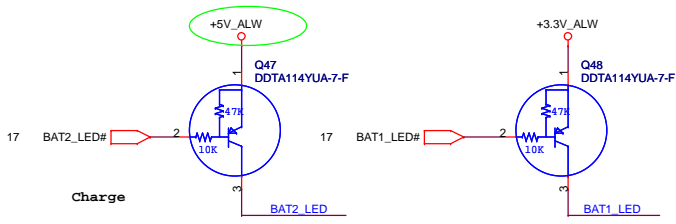
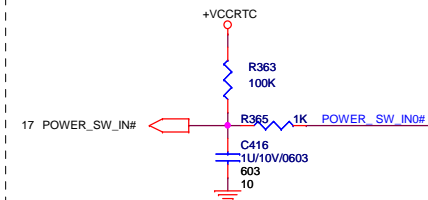
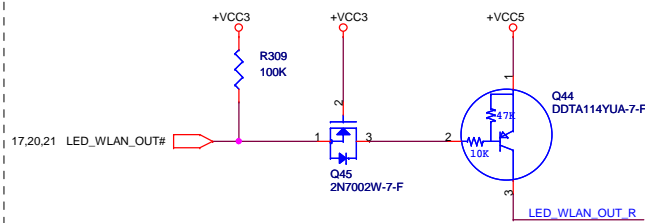
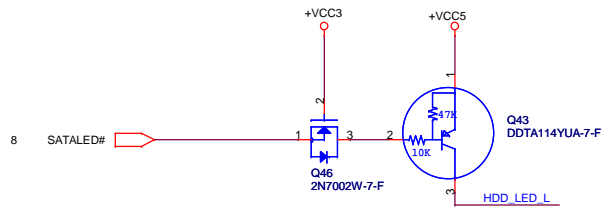
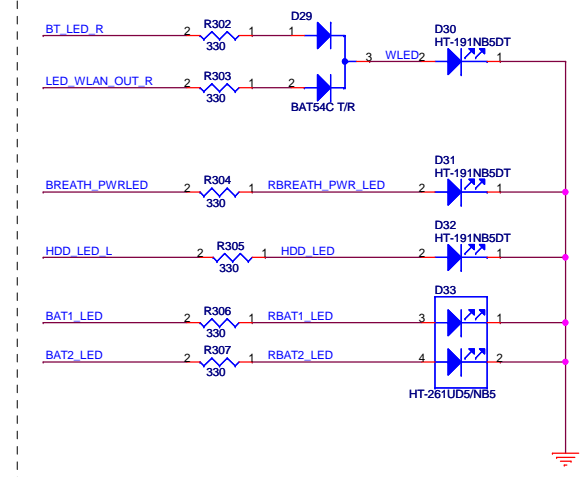
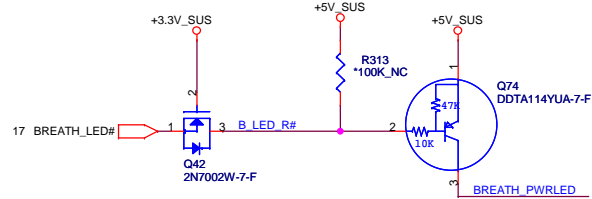
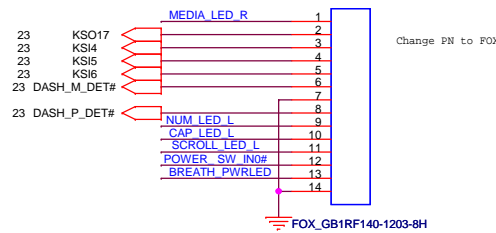
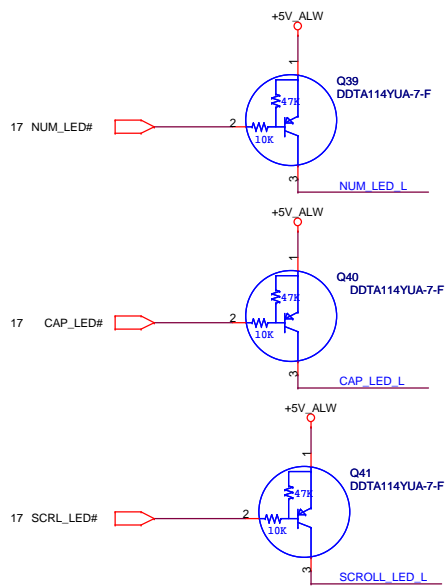
Internal Digital MIC move to LED Board



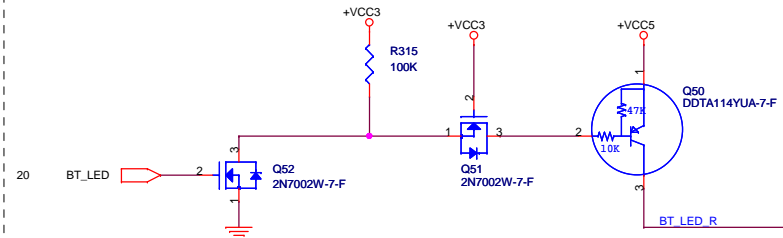
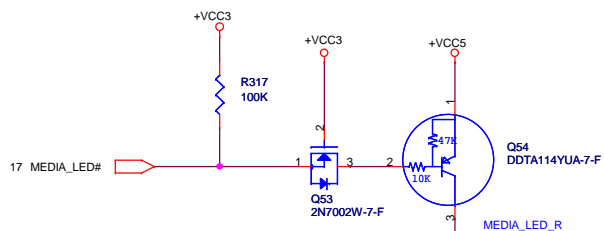
**JACK SENSE**



Title		CODEC	
Size	Document Number		Rev
	ZM2		D
Date	Wednesday, March 10, 2010	Sheet	28 of 43

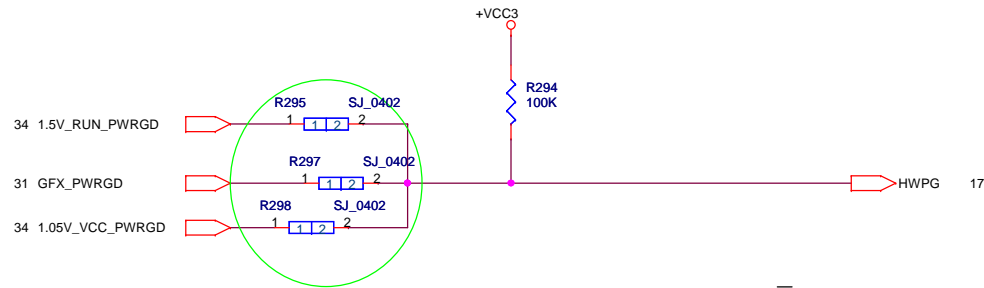



03/01 Change Q47 pin1 Power rail from +3.3V\_ALW to +5V\_ALW

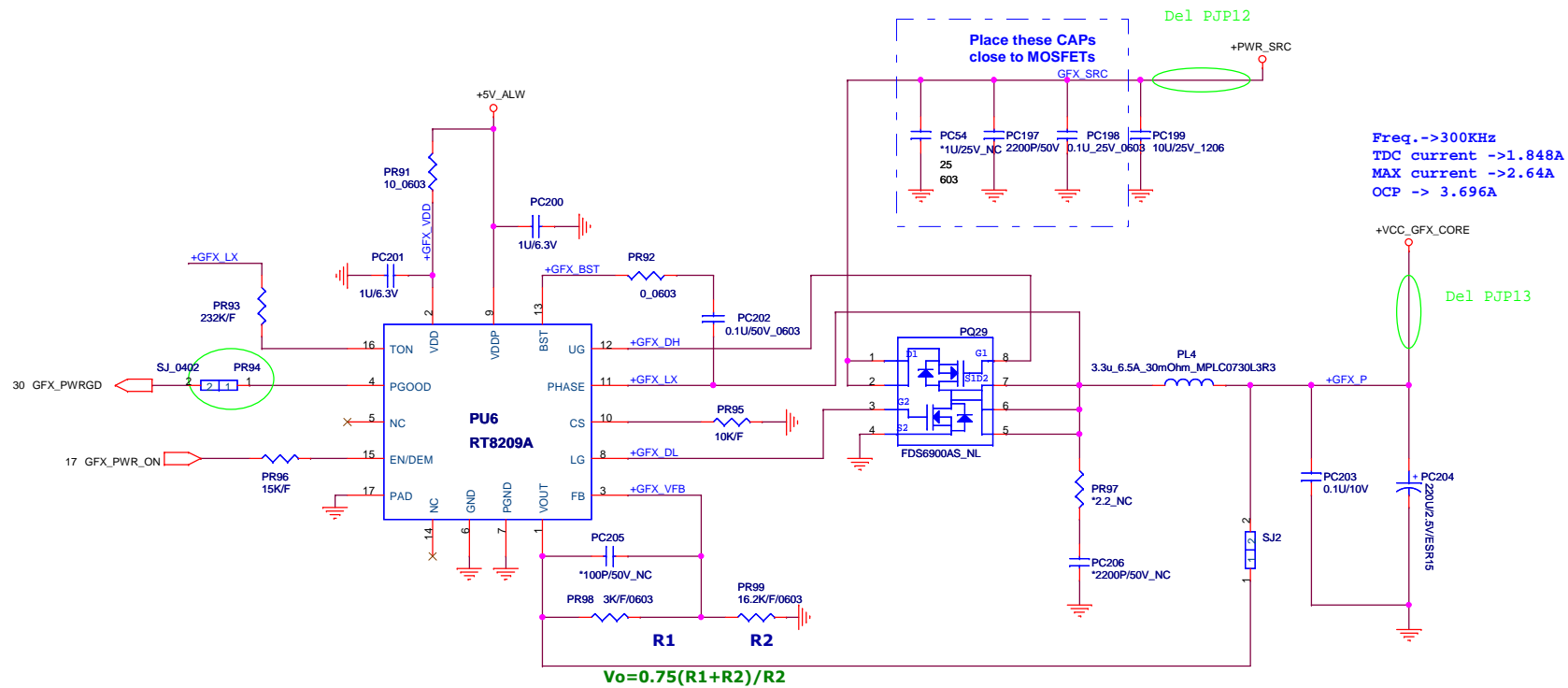


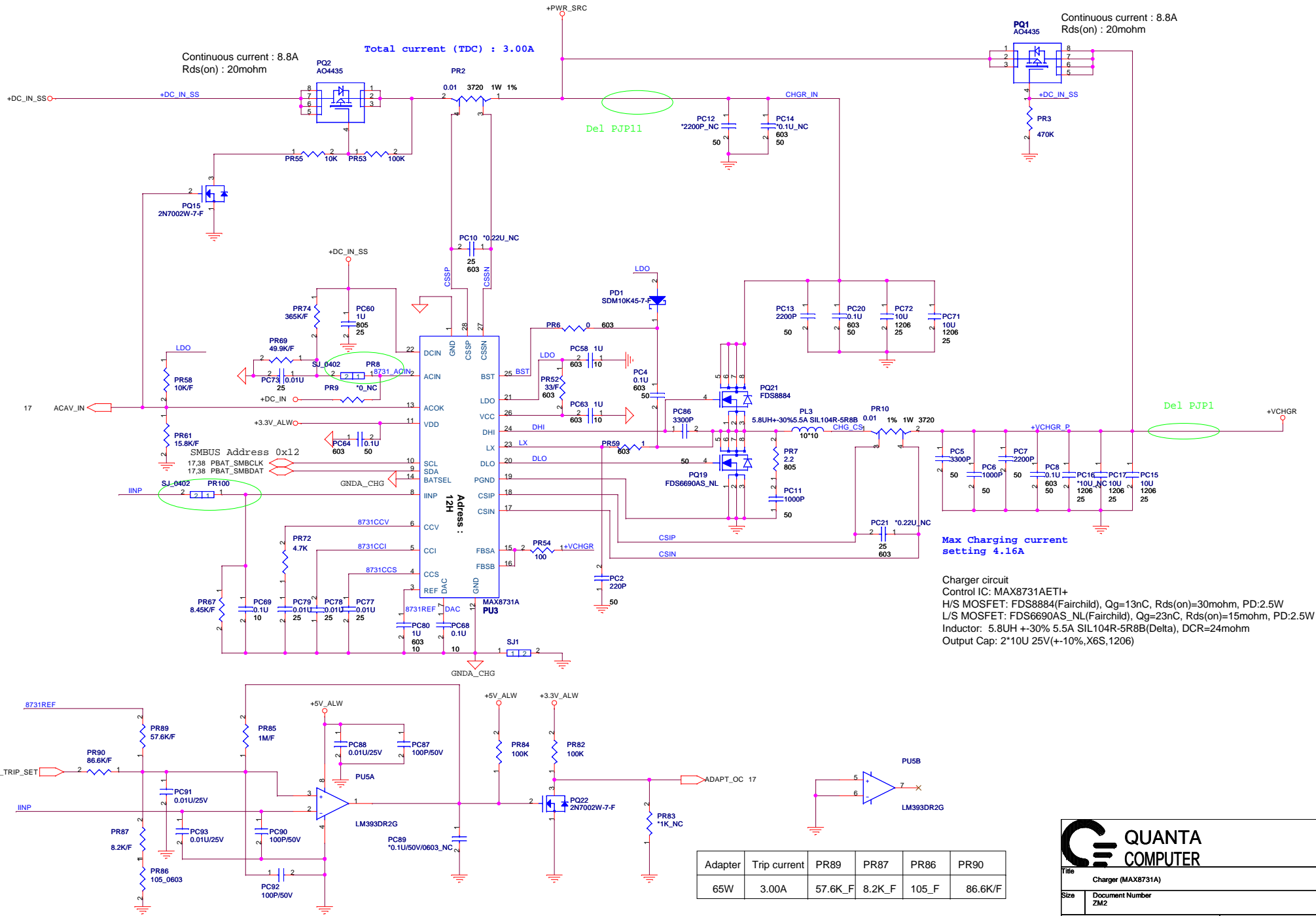
**QUANTA  
COMPUTER**

Title LED & SWITCH		
Size ZM2	Document Number ZM2	Rev D
Date: Wednesday, March 10, 2010	Sheet 29	of 43



 QUANTA COMPUTER			
Title System Reset Circuit			
Size	Document Number ZM2		Rev D
Date:	Wednesday, March 10, 2010	Sheet 30 of 43	





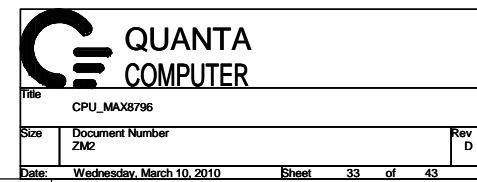
Charger (MAX8731A)

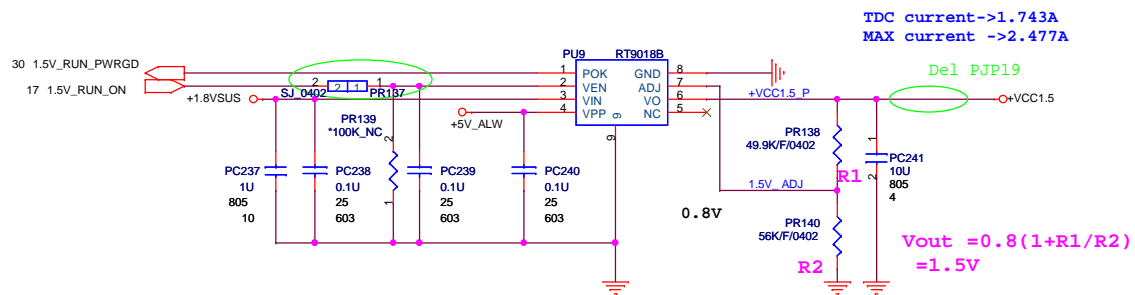
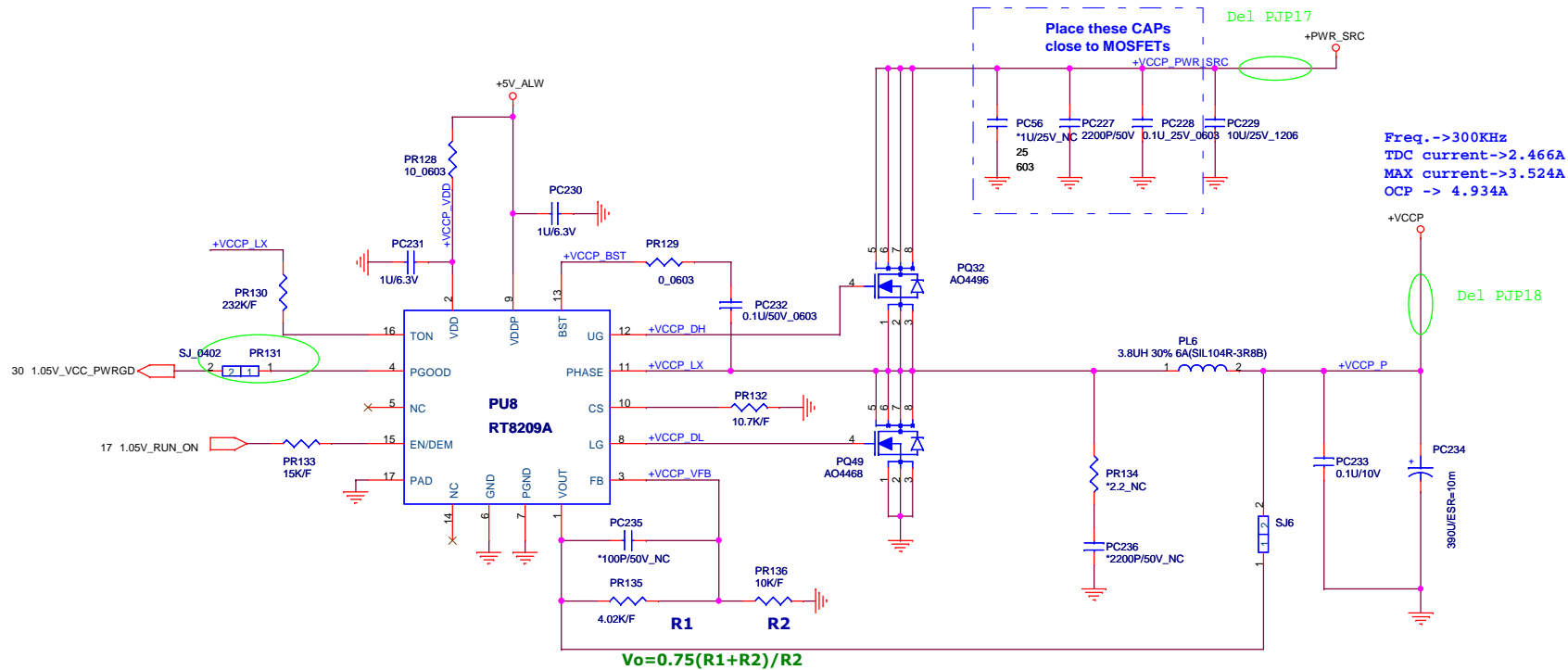
Size	Document Number	Rev
ZM2		D

Date: Wednesday, March 10, 2010 Sheet 32 of 43



TPU	GPU
TP1	CPU_VID0
TP2	CPU_VID1
TP3	CPU_VID2
TP4	CPU_VID3
TP5	CPU_VID4
TP6	CPU_VID5
TP7	CPU_VID6



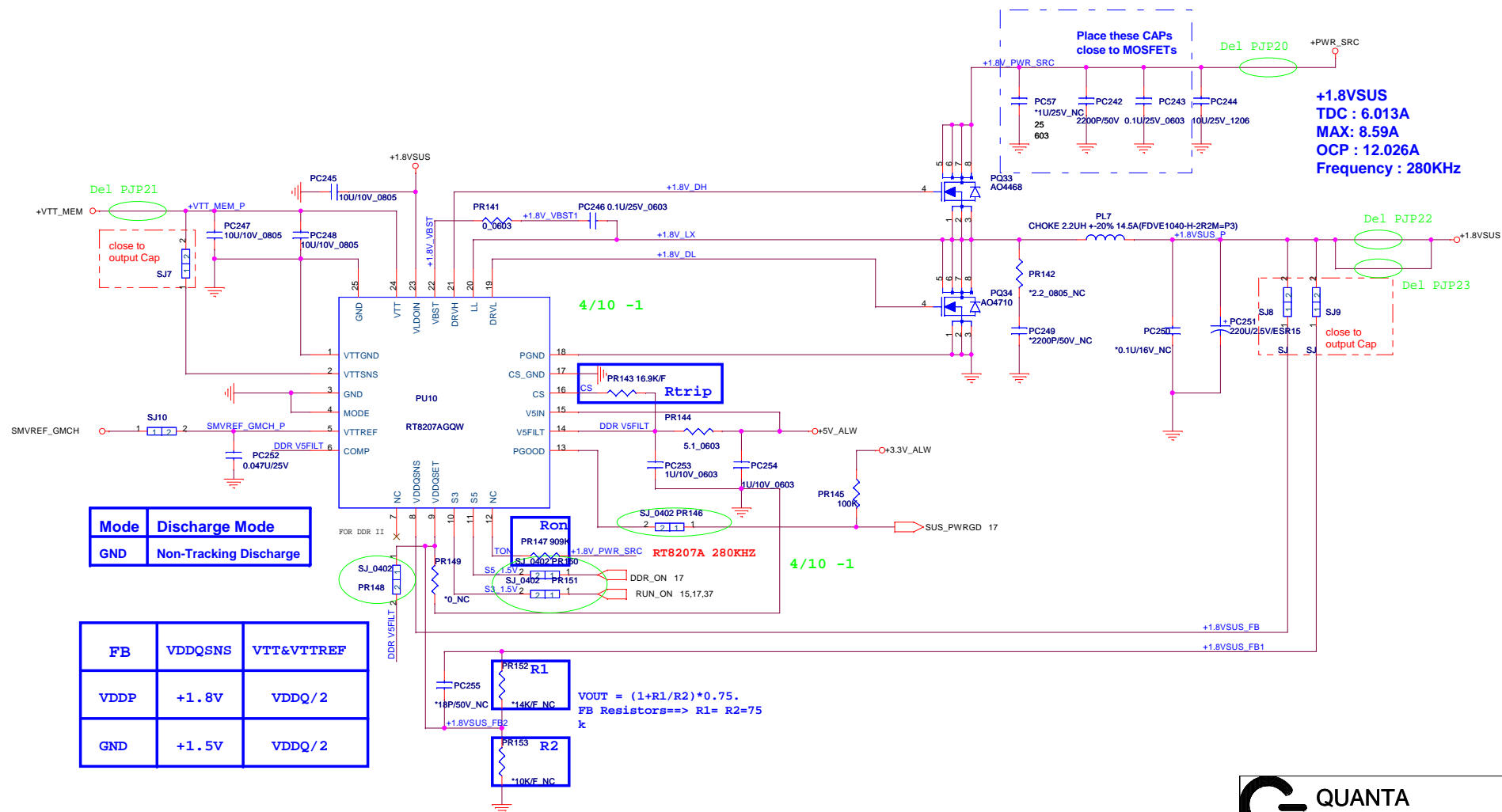


1.8V\_SUS power rail:  
Control IC: RT820TAGQW  
H/S MOSFET: AO4476, Qg=8.5nC, Rds(on)=17mohm, PD:3.7W  
L/S MOSFET: AO4710, Qg=15nC, Rds(on)=14.2mohm, PD:3.1W  
Inductor: 1.5UH +30%/12.5A(SIL1055RC-1R5-R)(Delta), DCR=7.6mohm  
Output Cap: 1\* 330U2.5V(20%, ESR9, 7343,H1.9)

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

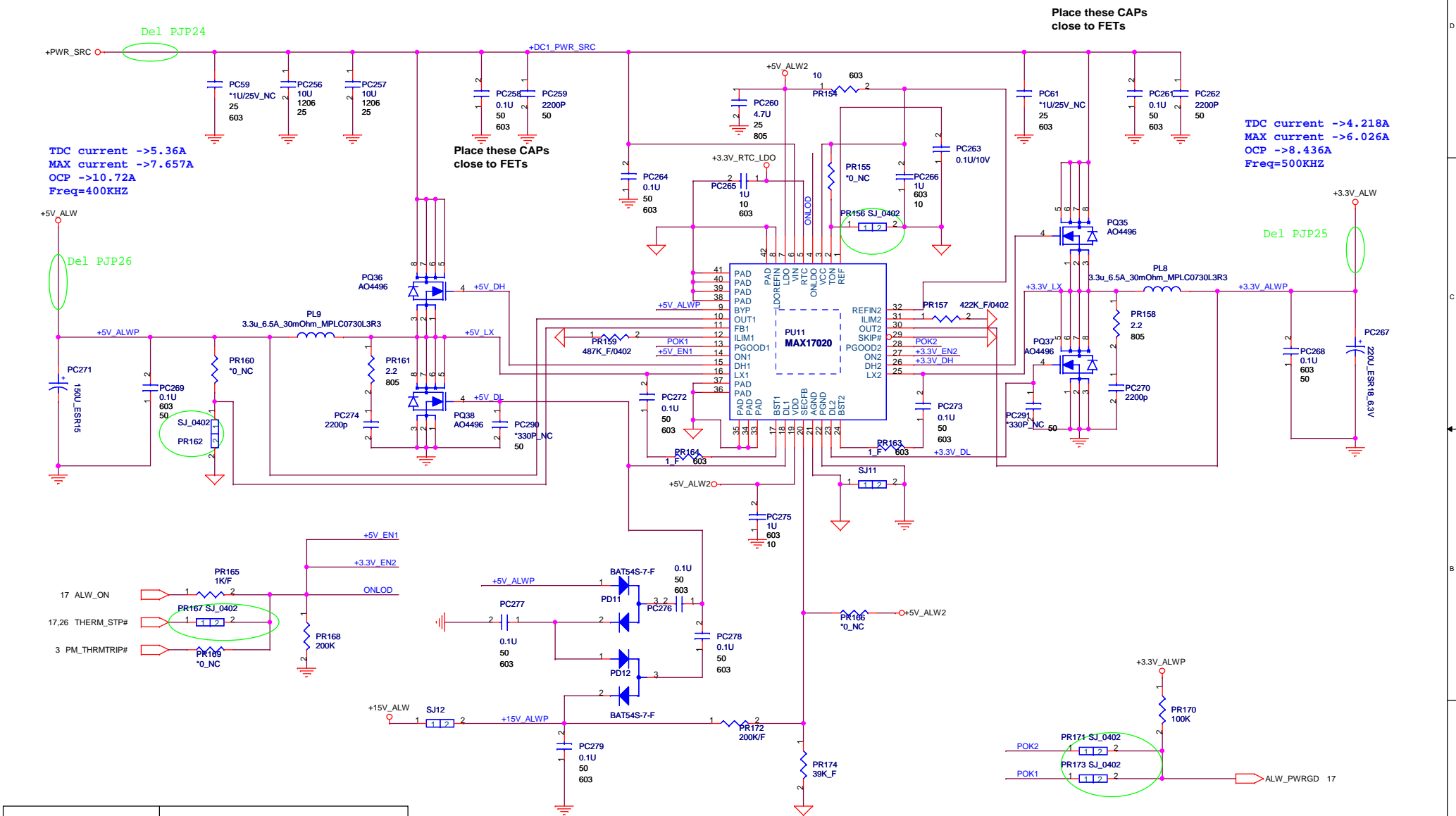
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)




5V\_ALW power rail:  
Control IC: RT8206B  
H/S MOSFET: AO4496, Qg=6.1nC, Rds(on)=26mohm, PD:3.1W  
L/S MOSFET: AO4496, Qg=6.1nC, Rds(on)=26mohm, PD:3.1W  
Inductor: 3.8uH 30% 6A(SIL104R-3R8B)(Delta), DCR=13mohm  
Output Cap: 1\* 330U,6.3V(20%ESR17,6.3\*5.8)

DC/DC +3V\_ALW/+5V\_ALW /+15V\_ALW

3.3V\_ALW power rail:  
Control IC: RT8206B  
H/S MOSFET: AO4496, Qg=6.1nC, Rds(on)=26mohm, PD:3.1W  
L/S MOSFET: AO4496, Qg=6.1nC, Rds(on)=26mohm, PD:3.1W  
Inductor: 3.8uH 30% 6A(SIL104R-3R8B)(Delta), DCR=13mohm  
Output Cap: 1\* 330U,6.3V(20%ESR17,6.3\*5.8)





QUANTA  
COMPUTER

Title

5V\_ALW, 3V\_ALW, 15V\_ALW

Size

Document Number

Rev

ZM2

D

Date:

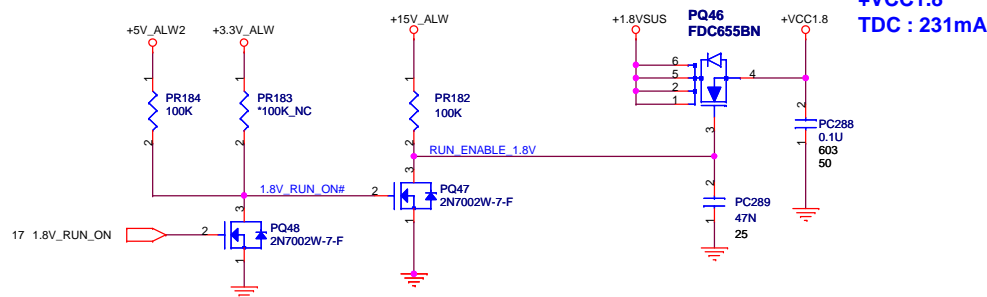
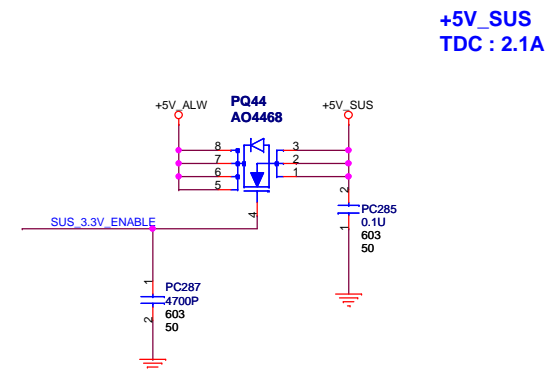
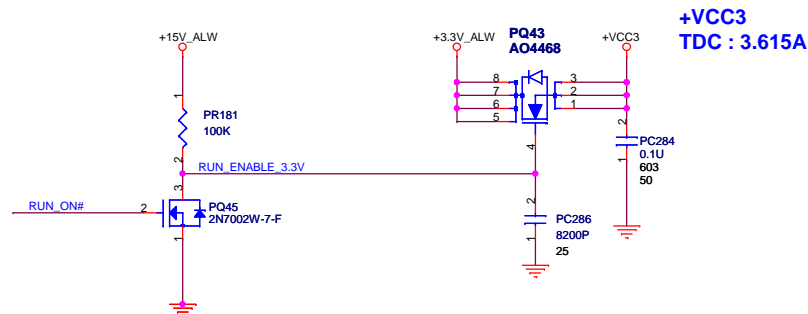
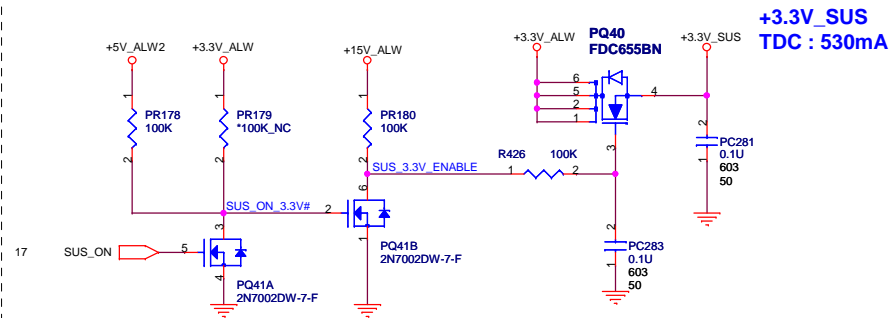
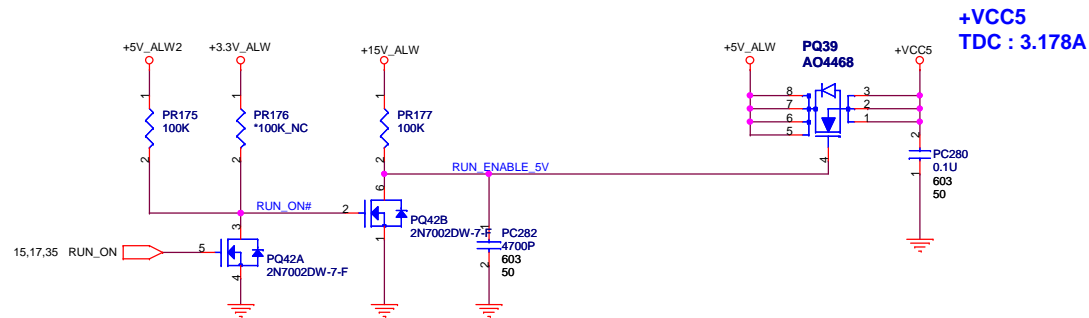
Wednesday, March 10, 2010

Sheet

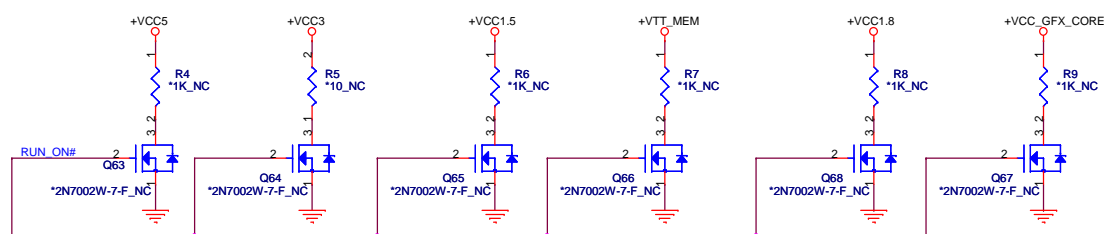
36

of

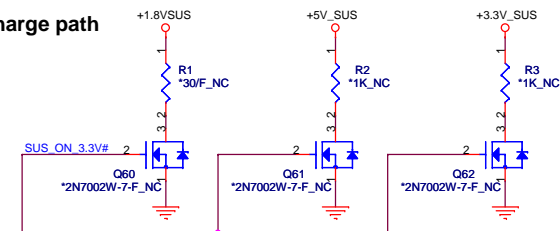
43



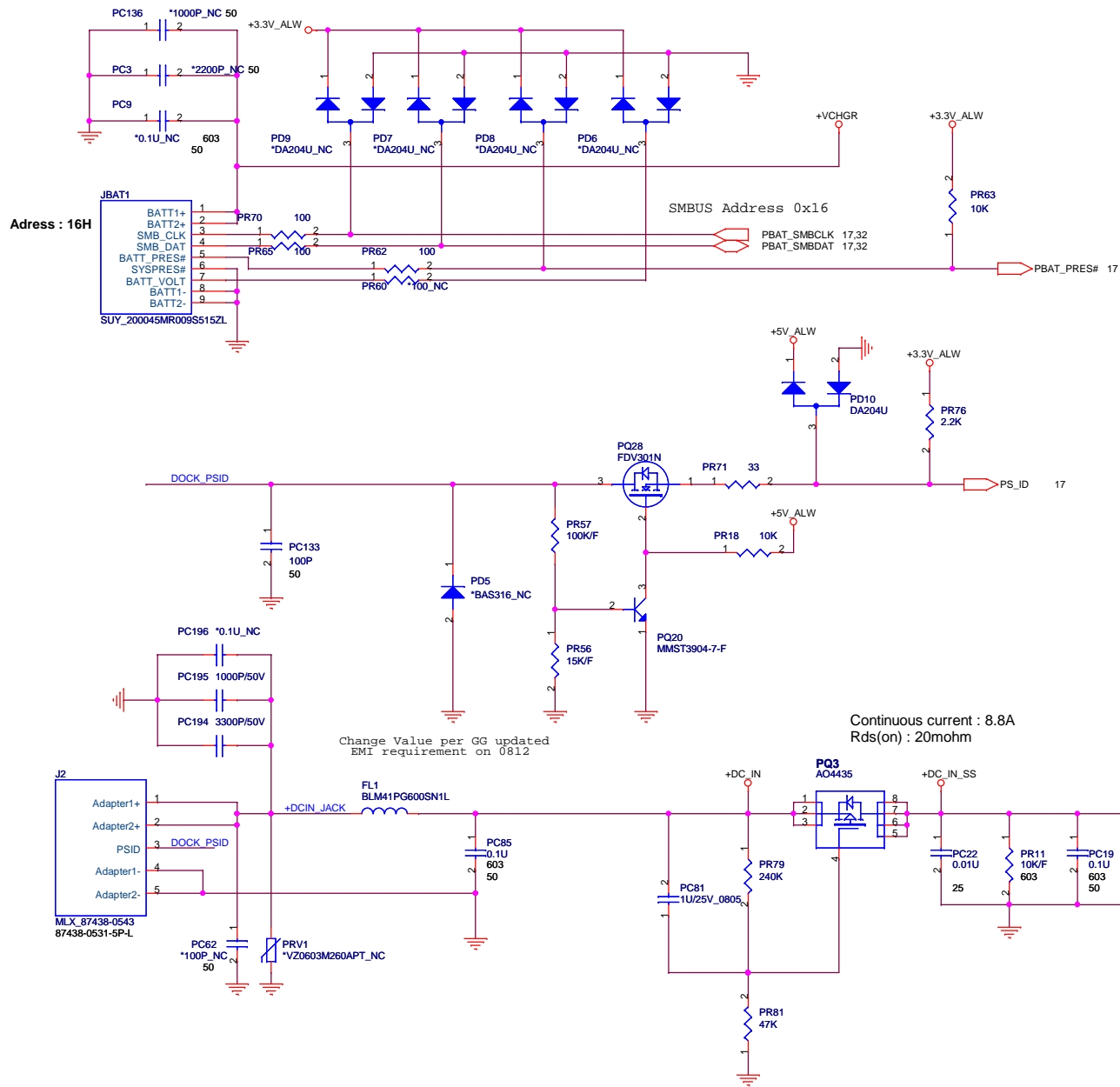
### Reserve discharge path



### Reserve discharge path



Title			RUN POWER SW
Size	Document Number	Rev	
	ZM2	D	
Date:	Wednesday, March 10, 2010	Sheet	37 of 43



Title  
DCIN,BATT CONNECTOR

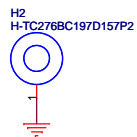
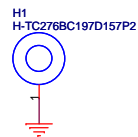
Size  
Document Number  
ZM2

Rev  
D

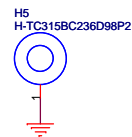
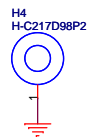
Date: Wednesday, March 10, 2010

Sheet 38 of 43

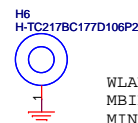
# H-TC276BC197D157P2



# H-TC315BC236D126P2

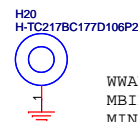


# H-TC217BC177D106P2



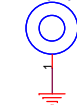
WLAN USE  
MBIM3001010  
MINI CARD NUT H16 IM3(MBIM3001,REV3A)CU

# H-TC217BC177D106P2

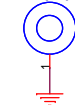


WWAN USE  
MBIM3001010  
MINI CARD NUT H16 IM3(MBIM3001,REV3A)CU

# H7 H-TC276BC197D169P2



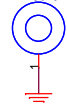
# H8 H-TC276BC197D157P2



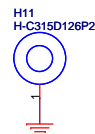
# H9 H-TC315BC236D39P2



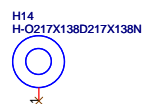
# H10 H-TC315BC236D98P2



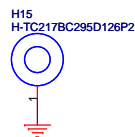
# H-C315D126P2



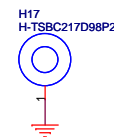
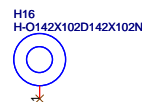
# H-C157D157N



# h-tc217bc197d126p2



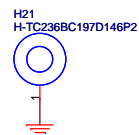
# h-c118d118n



# h-zm1-1

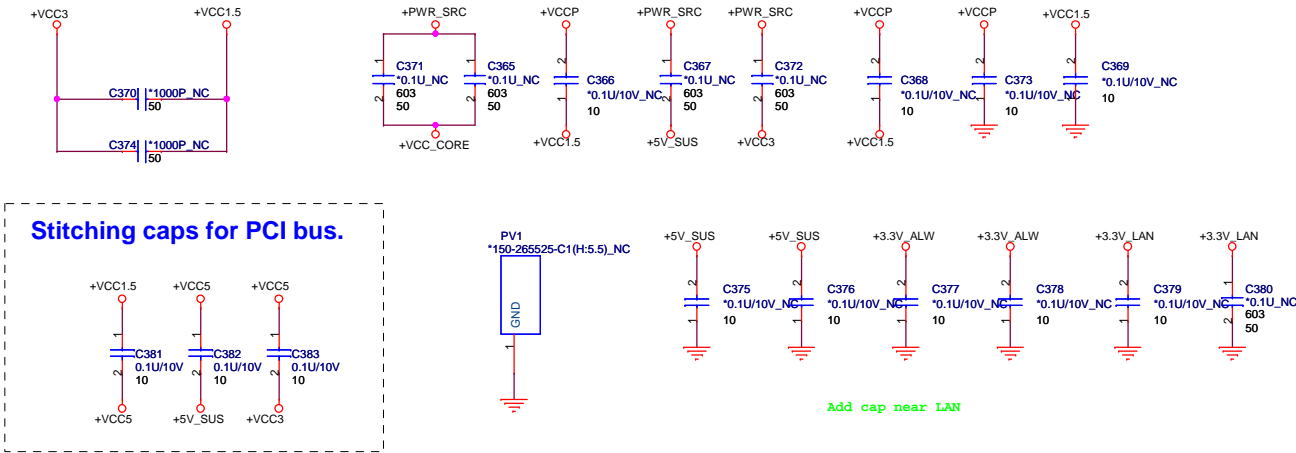


# H-C236D98P2

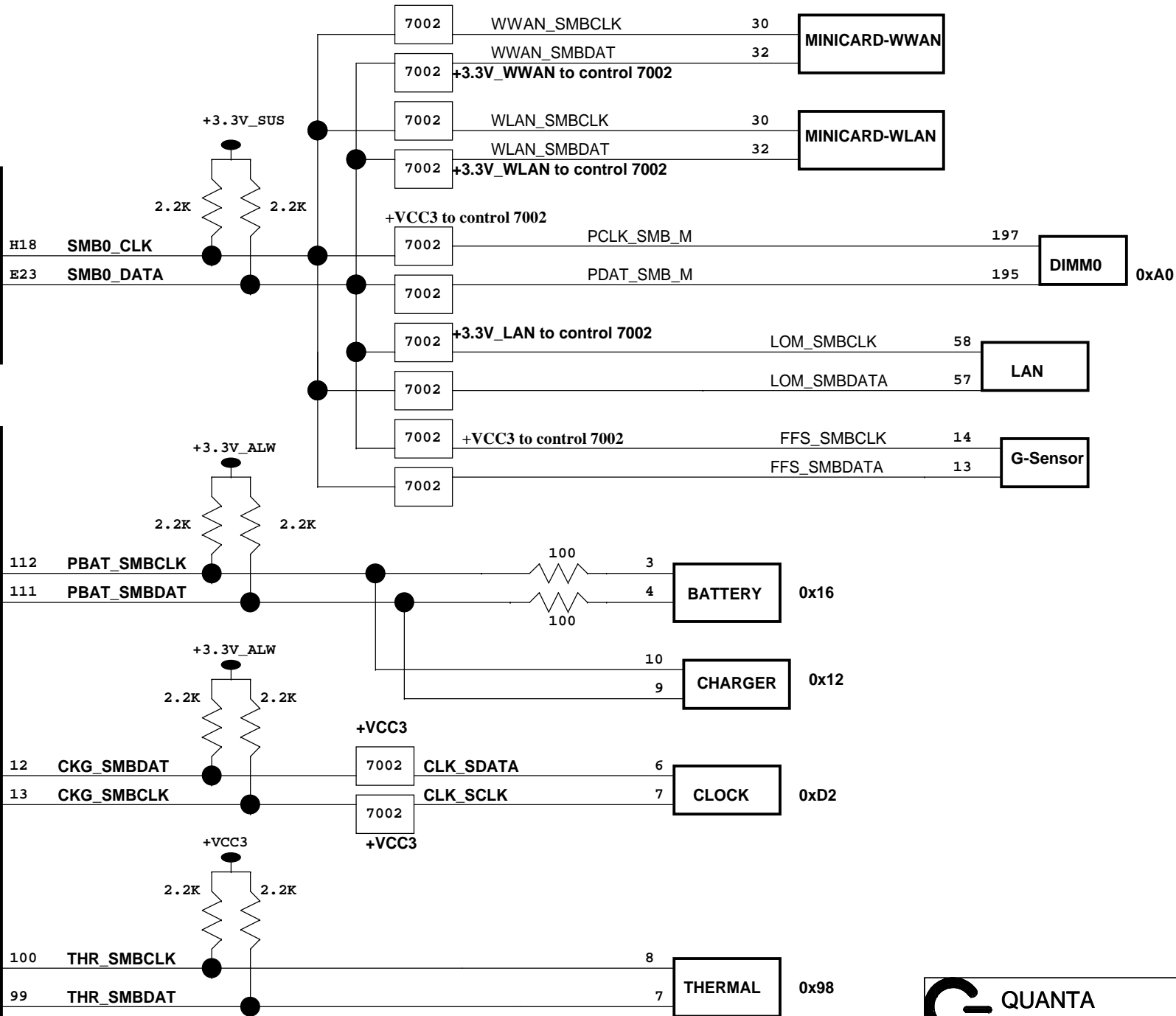
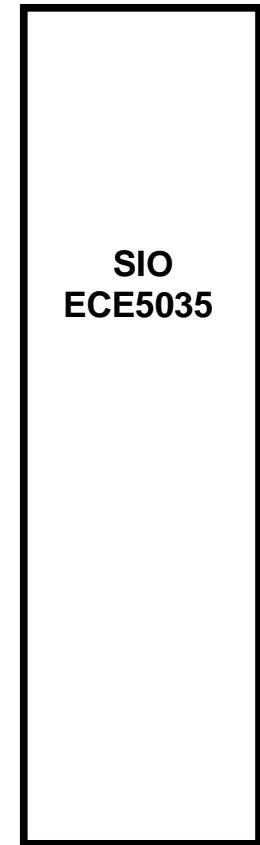
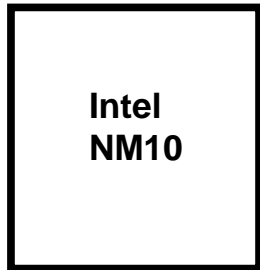


Reserved for EMI.

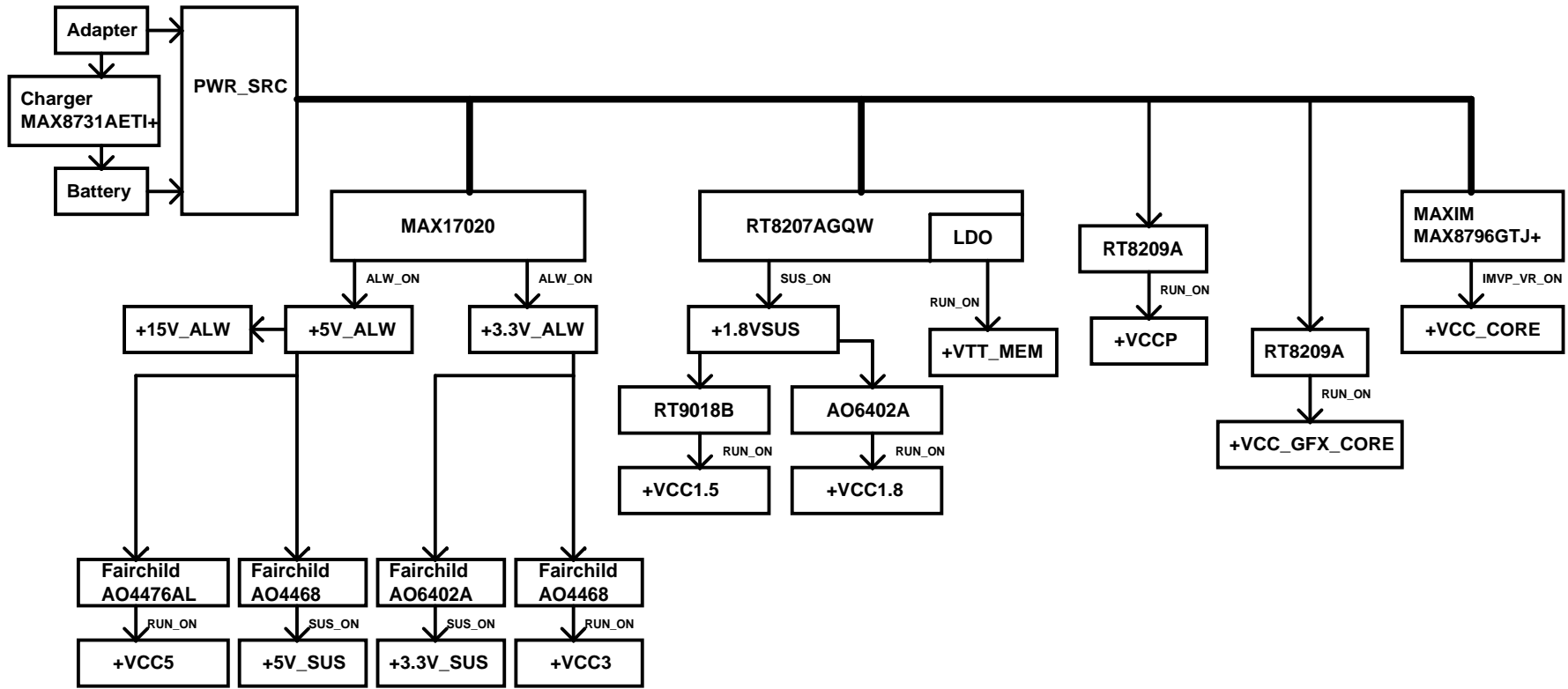
Stitching caps.







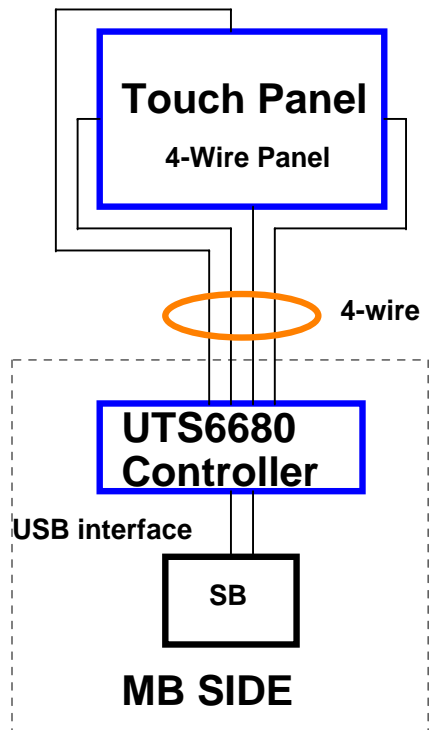
VER : 1A



USB Port#	Destination
USBP0	Right side top
USBP1	Right side bottom
USBP2	Left side
USBP3	Bluetooth
USBP4	Camera
USBP5	Touch Screen
USBP6	Mini WLAN
USBP7	Mini WWAN

PCI-E	Destination
PCIE-1	Mini WWAN
PCIE-2	Mini WLAN
PCIE-3	Card reader
PCIE-4	LAN

SATA	Device
SATA0	SATA/SSD HDD
SATA1	NC



AL006680B00IC OTHER(32P) UTS6680EF(LQFP)



Title Port Mapping			
Size	Document Number ZM2		Rev D
Date:	Monday, March 01, 2010	Sheet	43 of 43

[illegible]

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
ZM2	1	35	100125					Change PL7 P/N from DC-2282M000 to CV-22E5MZ00 Change PL7 footprint from CHOKE-MPLC0730L3R3 to CHOKE-MP0104-1R5

QUANTA

COMPUTER

Title

Change List

Size

Document Number

ZM2

Date

Monday, March 01, 2010

Sheet

2

of

2

Rev

D